A SerDes Balancing Act:
Co-Optimizing Tx and Rx Equalization Settings to Maximize Margin

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AGENDA

• Introduction
• Co-Optimization Examples
• How to Co-Optimize
• Summary
Why Co-Optimization?

- Increasing #links, data rates, and protocols
- EQ complexity / importance
  - PAM4, decreasing margin
  - Must balance Tx with Rx
- “Auto-Negotiation/Training” often isn’t
  - Good goal, will take time to achieve
- Problems not only loss
  - Traditional EQ targets loss
- Optimal settings: SW-only fix
  - Rescues failing links
Background

- Industry Paper
- Co-Optimization case study: performance 60%+, 25% longer
  - Compared with best-known EQ
  - Removed dozens of components
- Detail on Co-Optimization concepts and techniques
  - System-level Tx/Rx EQ tradeoffs
  - Refer to paper, big subject

This presentation illustrates Co-Optimization on a wider array of channels
EQ Concepts in Paper

- EQ recovers signals that disappeared
- Tx injects amplitude, which is good
  - And is the only source of pre-cursor EQ
- Most EQ removes amplitude, which is bad
  - Except DFE and some CTLEs
- Tx and Rx can trade post-cursor EQ
  - FFE and DFE taps, “co-optimize” adds CTLE
- All EQ except DFE affects multiple UI
- “Hula-Hoop” algorithm recovers clock
- Co-Optimization concepts are understandable
  - Basics can be applied manually

Well-suited for Automation?
AGENDA

• Introduction
• Co-Optimization Examples
  1. Manual Methods
  2. S-Parameter Channels
  3. Circuit-based Channels (NRZ & PAM4)
• How to Co-Optimize
• Summary
Co-Optimization Cockpit

- You can fly this plane
  - All examples available in SiSoft QCD Project file

- Co-Optimization = SiSoft OptimEye™ Technology
  - 3rd generation optimizer, Tx / Rx aware

- All variables adaptable
  - UI, EQ (FFE, DFE, CTLE), PCB Parameters, Jitter, Clock Recovery, etc.

*Details later in presentation...*
#1: Beat the Co-Optimizer?

- **Problem:**
  - Long/lossy channel
  - 4-tap Tx (1pre, 2post)
  - No Rx EQ
- **Manual Technique (blue):**
  - Force zero in all taps
- **OptimEye™ (red):**
  - Trade amplitude for ISI
  - 15% better eye
Equation-based & Iterative Methods

- Project has spreadsheets
- Either
  - Use paper’s equations to get close, then iterate
  - Or guess and iterate
  - Or both
- ~1 hour/tap, but can be done
  - Re-hula-hoop, estimate, repeat
- This resolves Tx EQ only
  - Tx/Rx EQ much more complex
Manual Sweep: Same Channel

• 2-step sweep of Tx taps
  1. coarse, ~500 runs, Statistical
  2. fine, ~500 runs, Statistical

• 1 hour, closer result
  – OptimEye 5% wider

• Results:

<table>
<thead>
<tr>
<th></th>
<th>Tap-1</th>
<th>Tap0</th>
<th>Tap1</th>
<th>Tap2</th>
<th>Eye</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hand_Calc</td>
<td>-0.07</td>
<td>0.54</td>
<td>-0.34</td>
<td>0.05</td>
<td>-15%</td>
<td>3 hours</td>
</tr>
<tr>
<td>Sweep</td>
<td>-0.08</td>
<td>0.59</td>
<td>-0.33</td>
<td>0.00</td>
<td>-5%</td>
<td>1 hour</td>
</tr>
<tr>
<td>OptimEye</td>
<td>-0.04</td>
<td>0.61</td>
<td>-0.35</td>
<td>0.00</td>
<td>Best</td>
<td>&lt; 1 sec</td>
</tr>
</tbody>
</table>
#2: S-Parameter Channels

Range of characteristics

- 7 Industry Channels
- 6 ISI Channels
- 6 Loss Channels
- 1 Failing Channel
Analysis Configuration

• Circuit
  – s4p channel, 10 Gbps
  – Advanced Tx/Rx w/ Dj, Rj, DCD

• SerDes EQ
  – 4-taps in Tx FFE and Rx DFE
  – Rx CTLE, 0-15, ~0-15dB boost

• EQ Preset Scenarios
  – 1: Tx taps ~half, CTLE=12
  – 2: Tx taps ~PCIe P7, CTLE=8
  – 3: OptimEye selects Tx / CTLE
  – Rx DFE always “auto”
Eye Height Results

- Typically 2x better
- Eyes for Channel 11:

![Eye Height vs Channel Type Graph](image)

- OptimEye™ PCIe P7
- Tx ½ Way
Eye Heights

Choose:

94% - Industry Channels

188% - ISI-Constrained Channels

53% - Loss-Dominated Channels

<table>
<thead>
<tr>
<th>Channel</th>
<th>1/2way</th>
<th>PCIe_P7</th>
<th>OptimEye™</th>
<th>Improved</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>s_1FCI_CC</td>
<td>0.104</td>
<td>0.137</td>
<td>0.202</td>
<td>47%</td>
<td>94%</td>
</tr>
<tr>
<td>s_2Comm</td>
<td>0.036</td>
<td>0.108</td>
<td>0.211</td>
<td>95%</td>
<td></td>
</tr>
<tr>
<td>s_3TEC_W</td>
<td>0.070</td>
<td>0.132</td>
<td>0.234</td>
<td>78%</td>
<td></td>
</tr>
<tr>
<td>s_4TEC_W</td>
<td>0.072</td>
<td>0.123</td>
<td>0.231</td>
<td>88%</td>
<td></td>
</tr>
<tr>
<td>s_5TX3_5</td>
<td>0.083</td>
<td>0.144</td>
<td>0.283</td>
<td>97%</td>
<td></td>
</tr>
<tr>
<td>s_6TX2_3</td>
<td>0.091</td>
<td>0.187</td>
<td>0.411</td>
<td>120%</td>
<td></td>
</tr>
<tr>
<td>s_7TEC_W</td>
<td>0.106</td>
<td>0.176</td>
<td>0.410</td>
<td>133%</td>
<td></td>
</tr>
<tr>
<td>s_Fail</td>
<td>0.006</td>
<td>0.003</td>
<td>0.007</td>
<td>163%</td>
<td></td>
</tr>
<tr>
<td>s_ISI1</td>
<td>0.001</td>
<td>0.024</td>
<td>0.068</td>
<td>177%</td>
<td></td>
</tr>
<tr>
<td>s_ISI2</td>
<td>0.001</td>
<td>0.023</td>
<td>0.118</td>
<td>413%</td>
<td></td>
</tr>
<tr>
<td>s_ISI3</td>
<td>0.048</td>
<td>0.110</td>
<td>0.254</td>
<td>131%</td>
<td></td>
</tr>
<tr>
<td>s_ISI4</td>
<td>0.049</td>
<td>0.118</td>
<td>0.262</td>
<td>122%</td>
<td></td>
</tr>
<tr>
<td>s_ISI5</td>
<td>0.071</td>
<td>0.143</td>
<td>0.329</td>
<td>130%</td>
<td></td>
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<tr>
<td>s_ISI6</td>
<td>0.072</td>
<td>0.162</td>
<td>0.416</td>
<td>156%</td>
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<tr>
<td>s_Loss1</td>
<td>0.018</td>
<td>0.063</td>
<td>0.072</td>
<td>13%</td>
<td></td>
</tr>
<tr>
<td>s_Loss2</td>
<td>0.021</td>
<td>0.064</td>
<td>0.087</td>
<td>36%</td>
<td></td>
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<tr>
<td>s_Loss3</td>
<td>0.003</td>
<td>0.053</td>
<td>0.086</td>
<td>64%</td>
<td></td>
</tr>
<tr>
<td>s_Loss4</td>
<td>0.021</td>
<td>0.071</td>
<td>0.098</td>
<td>38%</td>
<td></td>
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<tr>
<td>s_Loss5</td>
<td>0.025</td>
<td>0.081</td>
<td>0.137</td>
<td>70%</td>
<td></td>
</tr>
<tr>
<td>s_Loss6</td>
<td>0.031</td>
<td>0.091</td>
<td>0.179</td>
<td>96%</td>
<td></td>
</tr>
</tbody>
</table>
#3: Circuit-based Channels

- 10 Gbps, same EQ options and jitter as S-param channels
- Length: 12” to 47”, Lt_cd/bp: 0.015/0.009, ISI & Loss channels
- Permutations: 4 \( \text{bp}_{\text{len}} \times 3 \text{ rx}_{\text{len}} \times 2 \text{ bp}_{\text{via}} \times 2 \text{ rx}_{\text{via}} = 48 \)
- Total Simulations: 48 * 3 EQ options = 144
- Manufacturing tolerances
Passive Characteristics, 48 Channels

- Mix of ISI-Constrained & Loss-Dominated Channels
- 20 dB Insertion Loss variation at 5 GHz
Eye Height Results

- Similar trends
- Eyes for Channel 2:
## Eye Heights

**Improve:**

- **134%** - ISI-Constrained Channels

- **42%** - Loss-Dominated Channels

## Overall Averages:

- ISI: **145%**
- Loss: **44%**

### Table: Eye Heights (V) relative to PCIe_P7

<table>
<thead>
<tr>
<th>Channel</th>
<th>1/2way</th>
<th>PCIe_P7</th>
<th>OptimEye™</th>
<th><strong>Improved</strong></th>
<th><strong>Average</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.036</td>
<td>0.138</td>
<td>0.425</td>
<td>209%</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.006</td>
<td>0.085</td>
<td>0.348</td>
<td>310%</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0.072</td>
<td>0.174</td>
<td>0.380</td>
<td>119%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0.045</td>
<td>0.134</td>
<td>0.393</td>
<td>195%</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.052</td>
<td>0.123</td>
<td>0.317</td>
<td>157%</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0.016</td>
<td>0.090</td>
<td>0.195</td>
<td>117%</td>
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<tr>
<td>7</td>
<td>0.067</td>
<td>0.143</td>
<td>0.318</td>
<td>122%</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.033</td>
<td>0.107</td>
<td>0.224</td>
<td>110%</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0.033</td>
<td>0.099</td>
<td>0.184</td>
<td>86%</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>0.015</td>
<td>0.076</td>
<td>0.171</td>
<td>125%</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>0.042</td>
<td>0.108</td>
<td>0.212</td>
<td>95%</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0.021</td>
<td>0.084</td>
<td>0.190</td>
<td>127%</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>0.048</td>
<td>0.126</td>
<td>0.352</td>
<td>179%</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>0.012</td>
<td>0.084</td>
<td>0.279</td>
<td>233%</td>
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</tr>
<tr>
<td>15</td>
<td>0.074</td>
<td>0.157</td>
<td>0.383</td>
<td>144%</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>0.040</td>
<td>0.120</td>
<td>0.327</td>
<td>172%</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>0.040</td>
<td>0.109</td>
<td>0.239</td>
<td>118%</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>0.017</td>
<td>0.083</td>
<td>0.188</td>
<td>128%</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>0.053</td>
<td>0.124</td>
<td>0.254</td>
<td>106%</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>0.029</td>
<td>0.096</td>
<td>0.218</td>
<td>128%</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>0.028</td>
<td>0.087</td>
<td>0.149</td>
<td>71%</td>
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</tr>
<tr>
<td>22</td>
<td>0.014</td>
<td>0.070</td>
<td>0.112</td>
<td>60%</td>
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<tr>
<td>23</td>
<td>0.034</td>
<td>0.094</td>
<td>0.151</td>
<td>61%</td>
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</tr>
<tr>
<td>24</td>
<td>0.019</td>
<td>0.076</td>
<td>0.118</td>
<td>54%</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>0.025</td>
<td>0.088</td>
<td>0.180</td>
<td>106%</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>0.008</td>
<td>0.069</td>
<td>0.155</td>
<td>123%</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>0.040</td>
<td>0.106</td>
<td>0.200</td>
<td>89%</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>0.025</td>
<td>0.088</td>
<td>0.170</td>
<td>94%</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>0.023</td>
<td>0.076</td>
<td>0.112</td>
<td>47%</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>0.012</td>
<td>0.064</td>
<td>0.084</td>
<td>31%</td>
<td></td>
</tr>
</tbody>
</table>
PAM4

- Co-Optimization goes center-stage
  - Same OptimEye™ technology

- Channels 10”-18”

- Eye Height vs EQ
  - PCIe_P7
  - 10,80,10 + CTLE^ – OptimEye

- OptimEye™ 3x-5x improvement
  - Channel 3 eyes shown
AGENDA

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  – Manual Methods
  – S-Parameter Channels
  – Circuit-based Channels
• Using OptimEye™
• Summary
Using OptimEye™

- “QCD Optimization” attribute on any enabled Tx
- 2 modes – Tx & TxRx
- Runtime is longer than normal simulation

Answers in seconds instead of weeks

<table>
<thead>
<tr>
<th>Channels</th>
<th>Normal (s)</th>
<th>OptimEye™ (s)</th>
<th>x Longer</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 S-Parameter</td>
<td>38</td>
<td>62</td>
<td>1.6</td>
</tr>
<tr>
<td>48 Circuit-based</td>
<td>94</td>
<td>120</td>
<td>1.3</td>
</tr>
</tbody>
</table>

running TxRx mode, Statistical Analysis, Quad-core Laptop, Win7
What You Need to Know

• 3rd generation optimization technology
• Works with vendor AMI models
  – Control file enables optimization
  – Vendor models do not need to be recompiled
• Built-in support for SiSoft technology models
  – Determine if channels can be equalized
  – First-order EQ settings for vendor models
• Algorithms refined and proven through real-world use
Optimize Routed & Built Systems

Design

- Use OptimEye™ Pre- or Post-Route
- Single-board, or System of PCBs
- Actual routes refine design space

Debug

- Import / analyze failing channels
- Derive optimal settings
- Software change only
Firmware Settings: Optimize Each Channel

- OptimEye™ outputs derived settings to csv
- Depending on model, these are register values
  - Otherwise need to map
- Coordinate with firmware team to program
- Optimized performance and margins
Can You Beat the Co-Optimizer?

- Come by booth #935 to see if you can beat OptimEye™!

- SiSoft will be making this project available after DesignCon
AGENDA

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Summary

• **Co-Optimizing** Tx and Rx settings maximizes serial link performance
• “Blind sweeps” consume time and CPU cycles
• Analytical method is ideally suited for automation
• OptimEye™ technology provides
  – 100+% gains on ISI-Constrained channels
  – 50+% gains on Loss-Dominated channels
• Per-channel optimization is now practical at the full system level
QUESTIONS ?
THANK YOU