What Bumblebees and Models of DFE Have in Common

Michael Steinberger
Lead Architect, Serial Channel Products
SiSoft

While at first it may seem impossible or impractical to create an Input-output Buffer Information Specification, Algorithmic Modeling Interface (IBIS-AMI) model of Decision Feedback Equalization (DFE), it's actually quite easy as long as you understand some unavoidable artifacts in the results.

1.0 "It Can't Be Done"

Legend has it that aerodynamic analysis proves bumblebees can't fly. Similarly, there is a line of reasoning that proves that IBIS-AMI [1] [2] models of DFE can't possibly support statistical analysis, and cannot support time domain simulation of some popular DFE architectures.

Just as the (possibly apocryphal) aerodynamic analysis fails to account for the bumblebee wing's increased thickness (due to boundary layer thickness at low Reynolds number), and therefore its increased lift coefficient, there exist arguments about DFE models that are more focused on the problem than the solution.

This article will demonstrate how IBIS-AMI models can be written for some complex DFE architectures, and then demonstrate how such models can be written to support statistical analysis as well as time domain simulation.

2.0 Speculative DFE Architecture

The primary role of the IBIS-AMI specification is to define a standard interface to the model. While having a standard interface enables many solutions, it also imposes some constraints. One of those constraints is that the model has a single input and a single output for the primary data signal, with supplementary inputs and outputs only available for including crosstalk in statistical analysis. There are, however, many receiver architectures that have multiple data paths, with the detected data selected from the outputs of these paths. How can IBIS-AMI modeling represent such architectures?

The speculative DFE architecture has been used for a number of years, and is a good example of the challenges posed by multiple data paths. In the speculative DFE

architecture, there are two data paths that receive the same incoming data signal but apply equal and opposite low-frequency offsets to that signal. The magnitude of this offset is equal to the value of the first DFE tap. Both data paths make a decision at every bit time, but then the data bit delivered downstream is selected based on the previously detected bit. If the previously detected bit was a one, then the result from the negative offset data path is chosen. And if the previously detected bit was a zero, then the result from the positive offset data path is chosen.

The advantage of the speculative DFE architecture is that it is not necessary to feed the detected data bit back to the decision circuit input in time for the detection of the very next data bit. Instead, the choice of detected bit is deferred for one bit time, therefore providing a lot more timing margin in the circuit, at the expense of some duplication of circuitry.

To avoid complicating the example, Figure 1 illustrates the operation of a speculative DFE receiver with a single tap. In Figure 1, the magenta waveform is the incoming data signal, the blue waveform is the incoming data signal offset in the positive direction by the DFE tap and the yellow waveform is the incoming data signal offset in the negative direction by the DFE tap. This figure also shows markers for the edges of some of the data symbols. The data will be detected halfway between these markers.

Ideally, a model of this architecture would maintain both the positive and negative offset data paths and choose between them just the way

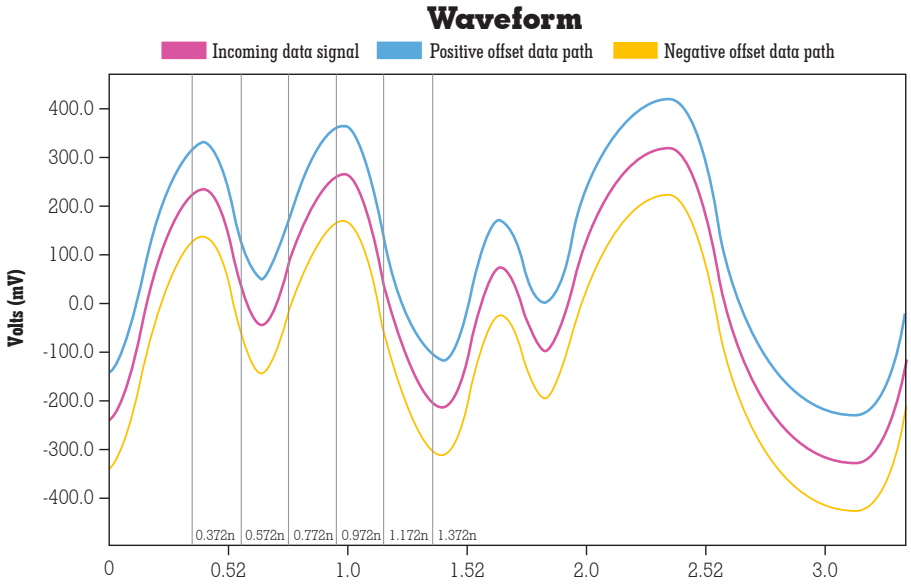

Figure 1: Speculative DFE Operation

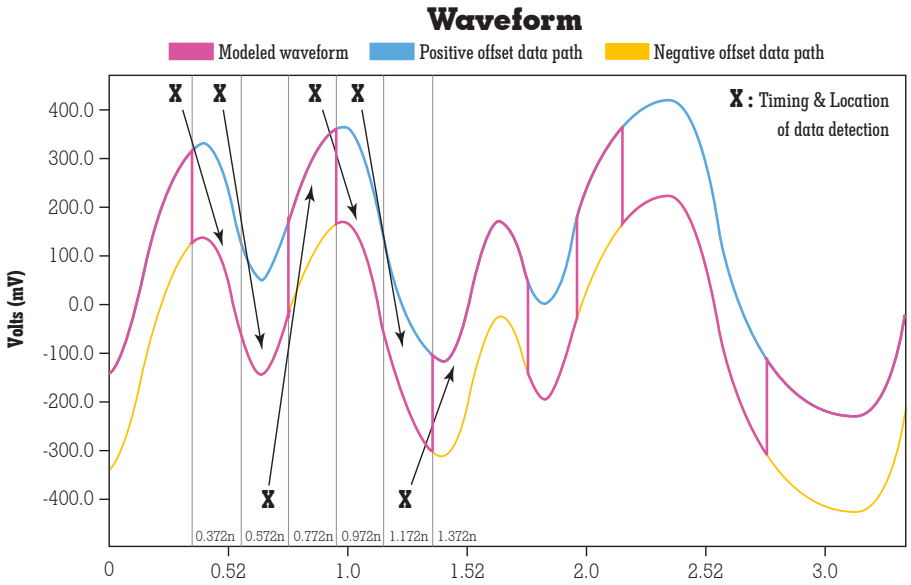

Figure 2: Speculative DFE Modeling

the real receiver does. The IBIS-AMI model interface will not support this. For any given bit, however, all that really matters is the value of the waveform that will actually be used to detect the value that will be delivered downstream. The model is capable of determining, for each bit, which of these two waveforms will be used, and is therefore able to deliver the pertinent waveform segment for each bit. This is illustrated by the magenta waveform in Figure 2. Each detected data bit determines which waveform segment will be output for the next bit.

Figure 3 is the eye diagram that was produced from the model's output waveform in Figure 2. Note that the

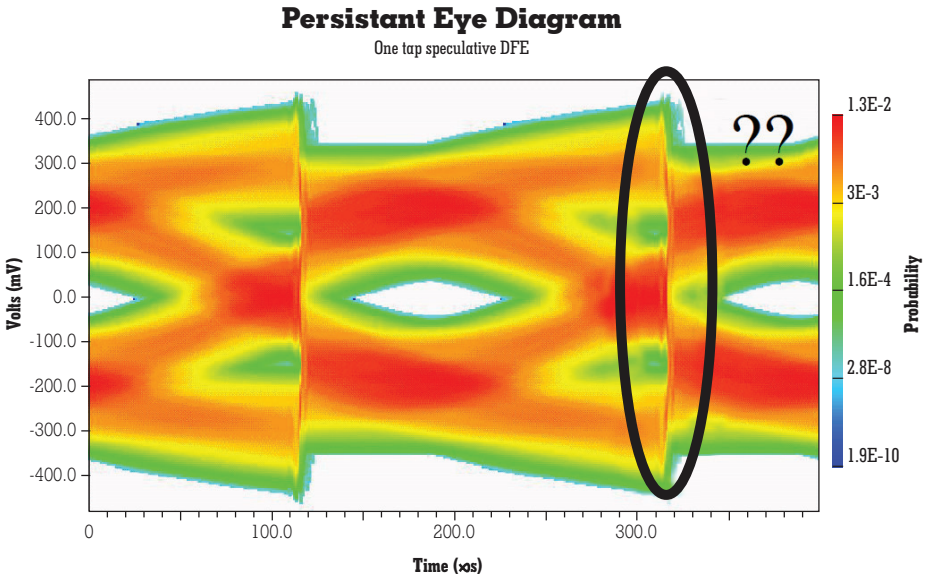

Figure 3: Speculative DFE Eye Diagram

middle of this eye diagram looks like an eye diagram that would be measured in the lab, but that the discontinuities in the model's output waveform are clearly evident at the edge of the eye. Every model is an illusion to some extent, and in this case the illusion only works in the center of the eye.

Because the values that affect the bit error rate analysis are taken from the center of the eye and not the edge, the discontinuity at the edge of the eye is not relevant. If, however, one were to perform a jitter analysis based on this waveform, then the discontinuities in the model's output waveform would render the results completely invalid. If a jitter analysis is to be performed, it should be performed on the model's clock output and not its output data waveform.

3.0 Statistical Analysis

In order to be rigorously valid, statistical analysis must use the response of a linear, time-invariant system. The input to a DFE tap is the output of the data detector, which is nonlinear. Furthermore, DFE is usually controlled by a continuously operating control loop. Therefore the tap weight is time-varying. So DFE is neither linear nor time-invariant. One would therefore conclude that statistical analysis in not applicable to a link that has DFE.

Consider the following assertions, however:

1. In steady state operation, the taps weights of a DFE are essentially constant.
2. The transmit amplitude of a high-speed serial channel is essentially constant.
3. In normal or expected operation, the receiver bit error rate is very low.

We define the following symbols:

x(t): The data signal driving the channel

y(t): The signal at the receiver's data decision point

z(t): The output data from the receiver

hc(t): The impulse response of the channel including any transmit equalization and any receiver linear equalization

wk: The k-th DFE tap weight

T: Transmit symbol duration

Tc: Channel delay

Then the signal at the receiver decision point is the sum of the linear channel/equalization response plus the DFE signal:

$$y(t) = h_c(t) \otimes x(t) + \sum_{k=1}^{n} w_k z(t - n\tau) \quad \text{(EQ1)}$$

The third assertion implies

$$z(t) = x(t - \tau_c) \quad \text{(EQ2)}$$

Substituting Equation 2 into Equation 1,

$$y(t) = h_c(t) \otimes x(t) + \sum_{k=1}^{n} w_k x(t - n\tau - \tau c) \quad \text{(EQ3)}$$

Employing the Dirac delta function $\delta(t)$,

$$y(t) = h_c(t) \otimes x(t) + \sum_{k=1}^{n} w_k \delta(t - n\tau - \tau c) \otimes x(t) \quad \text{(EQ4)}$$

$$y(t) = \left(h_c(t) + \sum_{k-1}^{n} w_k \delta(t - n\tau - \tau_c \right) \otimes x(t) \quad \text{(EQ5)}$$

Note that Equation 5 appears to be a linear, time-invariant equation in which the DFE taps are represented as Dirac delta functions. The equation is not rigorously linear

in that it's only valid if the transmit and receive data have the same amplitude and the bit error rate is low. Nonetheless, these assertions are true under a wide enough range of conditions that this equation is a useful engineering approximation.

Reference [2] gives more of the details on the practical application of this modeling approach. For the example given in the previous section, Figure 4 shows the impulse response of the end-to-end channel and Figure 5 shows the statistical eye diagram.

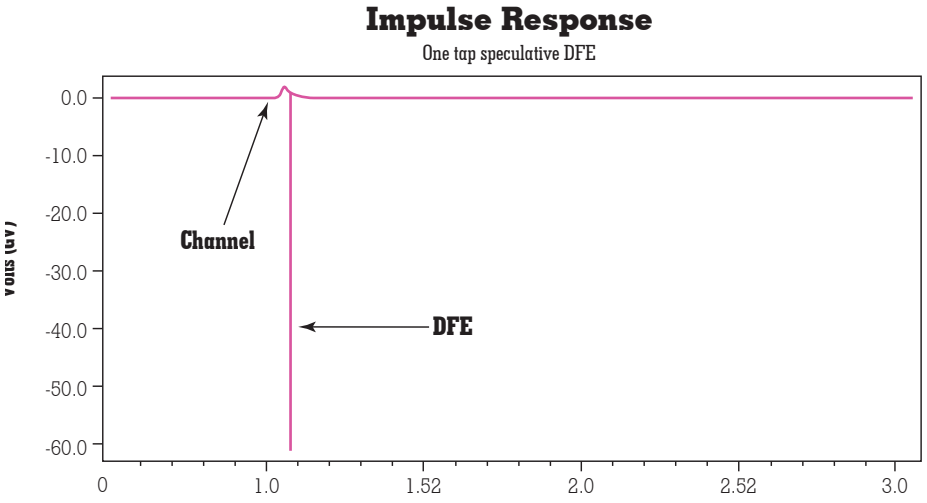

Figure 4: Impulse response with single tap DFE

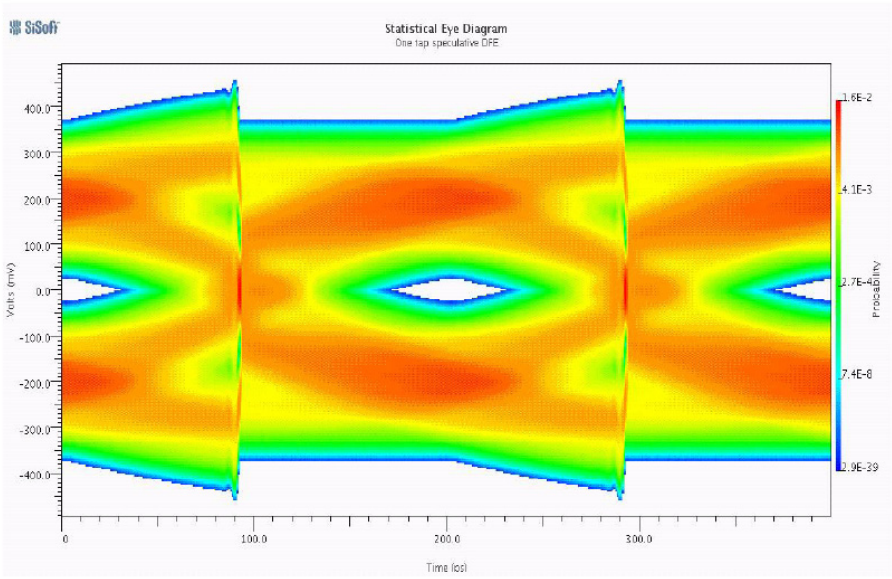

Figure 5: Statistical eye diagram with DFE

4.0 Conclusion

Bumblebees do fly, and IBIS-AMI models of DFE, correlated with measured data, are used routinely to produce accurate performance estimates for high-speed serial channels. The only caveat is that users need to understand the limitations of the model and therefore need to ignore the discontinuity at the edge of the eye diagram.

5.0 References

[1] IBIS (I/O Buffer Information Specification) Version 5.0, August 29, 2008.

[2] Michael Steinberger, Todd Westerhoff, Christopher White, "Demonstration of SerDes Modeling using the Algorithmic Model Interface (AMI) Standard", DesignCon2008, paper 7-TA3, February 5, 2008.

About the Author

Michael Steinberger, Ph.D., is responsible for leading SiSoft's ongoing tool development effort for the design and analysis of serial links in the 5-30 Gbps range. Dr. Steinberger has over 30 years experience in the design and analysis of very high speed electronic circuits. Dr. Steinberger began his career at Hughes Aircraft designing microwave circuits. He then moved to Bell Labs, where he designed microwave systems that helped AT&T move from analog to digital long-distance transmission. He was instrumental in the development of high speed digital backplanes used throughout Lucent's transmission product line. Prior to joining SiSoft, Dr. Steinberger led a group of over 20 design engineers at Cray Inc. responsible for SerDes design, high speed channel analysis, PCB design and custom RAM design. ■