

Using IBIS-AMI Models to Study Clock Recovery Loop Performance

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Abstract— Clock recovery loop behavior can seriously affect the performance of a high speed serial channel, and yet very little definitive data is available on the performance of the clock recovery loops in SerDes macros. This paper introduces a method for extracting the jitter transfer function and pattern dependent jitter from an IBIS-AMI model under realistic channel conditions, and presents example results from a generic bang-bang clock recovery design and seven commercial SerDes designs.

Keywords— High Speed Serial Channels, Clock Recovery, IBIS-AMI Modeling, Performance Analysis, Jitter Analysis

I. PROBLEM

There are several approaches to estimating the bit error rate of a high speed serial link. One approach is jitter-based analysis. (See, for example, [1].) The underlying hypothesis is that an error will occur whenever the clock to data timing at the decision latch is violated, and so the goal of the analysis is to estimate the probability density function (PDF) of the clock to data timing.

Another approach is to treat the bit error rate estimate as a conditional probability calculation. (See, for example, [2].) The probability of error given a constant clock to data timing is estimated for each possible clock to data timing, resulting in a conditional probability curve. The clock to data timing is then assumed to be independent of the data, and the probability of error is estimated by evaluating the integral of the conditional probability times the PDF of the clock to data timing.

In either case, the clock to data timing is central to the calculation. Since the clock is provided by a clock recovery loop, the jitter transfer function, jitter injection, and pattern dependent jitter of the clock recovery loop directly affects the bit error rate.

Furthermore, most clock recovery loops depend on a reference clock. The reference clock has some amount of phase noise with respect to an ideal reference, and the jitter injection of the clock recovery loop is determined by the reference clock phase noise as filtered by the clock recovery loop jitter transfer function.

Unfortunately, most SerDes suppliers do not provide performance data for the clock recovery loop, and so serial link

performance must be estimated using less specific information, making the performance estimate much less reliable. For example, there is no reliable way to estimate the pattern dependent jitter as a function of transmission path and equalization solution. Also, the design of the reference clock distribution network can affect the performance of the serial link, and yet critical data needed to include the reference clock phase noise in the performance analysis is missing.

II. METHOD

IBIS-AMI (I/O Buffer Information Specification – Algorithmic Modeling Interface) models [3], [4] provide a mechanism for determining the behavior of a clock recovery loop. When used in a time domain simulation, the IBIS-AMI model of a receiver can produce an array of times at which the edges of the recovered clock occur. If the IBIS-AMI model was written to accurately represent the architecture of the clock recovery loop, then the contents of this so-called `clock_ticks` array is a direct representation of the behavior of the clock recovery loop.

As will be demonstrated in this paper, the transmission path and equalization solution directly affect the behavior of the clock recovery loop. The fundamental reason is that intersymbol interference causes the data timing to vary, and so intersymbol interference reduces the sensitivity of the phase detection, regardless how that detection is implemented.

Thus, clock recovery loop behavior must be evaluated in the context of realistic channel conditions. It is therefore more difficult to introduce a known stimulus with which to measure the response. The solution is to introduce a known amount of random jitter (RJ) into the transmitted signal and measure how much of that jitter is evident in the `clock_ticks` at the output of the receiver. Since this operation is performed in a simulator, the actual jitter values injected into the signal are known, and so it is possible to obtain the phase as well as the magnitude of the jitter transfer function. It is assumed that the jitter transfer is a linear process, and so the calculation is a deconvolution of the `clock_ticks` with respect to the transmitted RJ.

The phase noise at the output of the clock recovery loop will contain pattern dependent jitter in addition to the phase noise due to the transmitted RJ. Since the pattern dependent jitter is uncorrelated with respect to the RJ, however, it can be

averaged out over a large number of bits. Ten million bits of time domain simulation produce usable results, but one hundred million bits are required to produce results that look relatively clean.

It is also possible to obtain the spectral density of the pattern dependent jitter, either by simulation without injecting RJ in the transmitted signal, or by using the jitter transfer function to calculate the output jitter that was due to the transmitter RJ and subtracting that from the total. The results in this paper were generated using the latter approach.

III. RESULTS

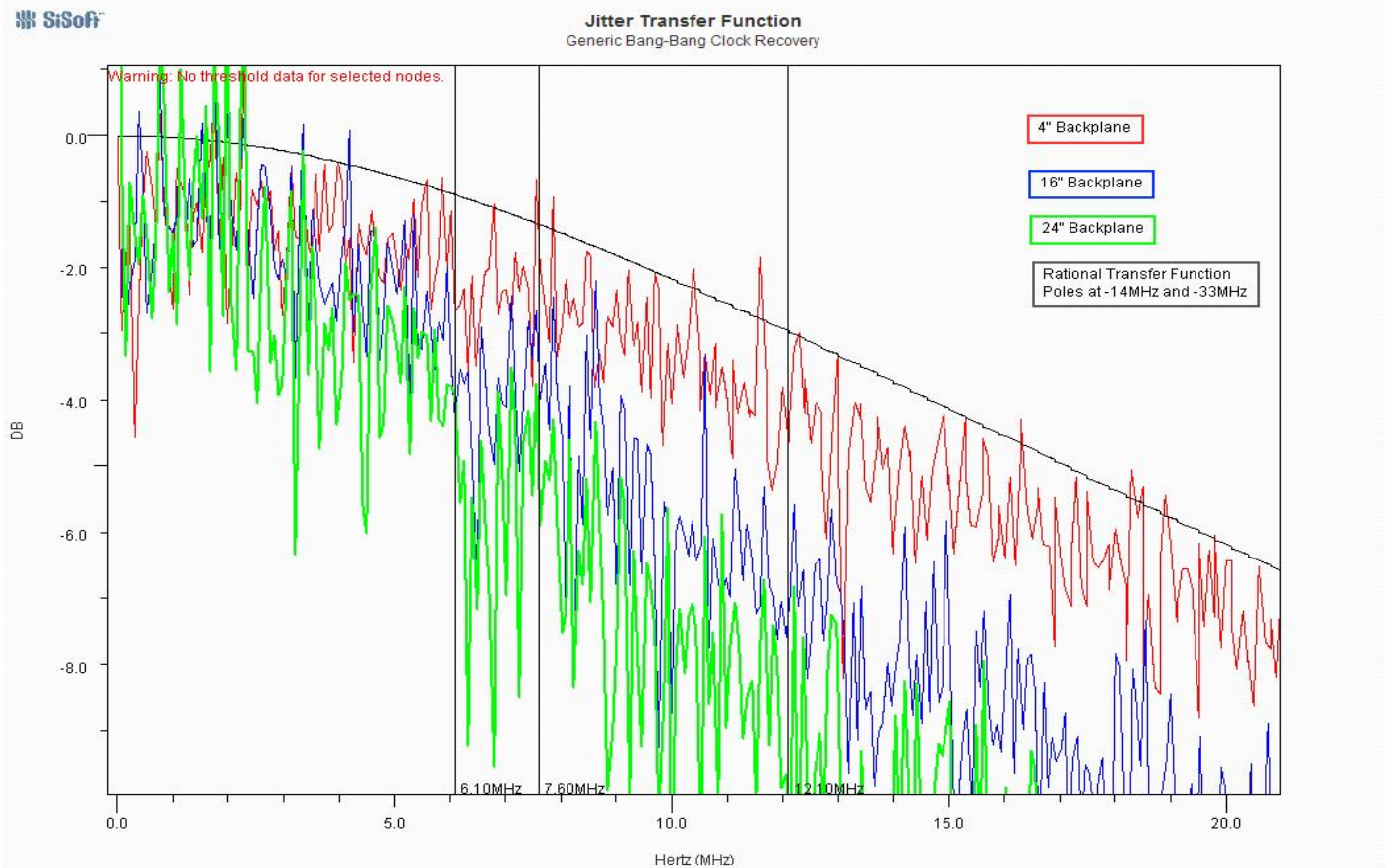
SiSoft supplies a model of a bang-bang clock recovery loop as part of a generic receiver model [4]. We used this model with the same XAUI-HM-Zd transmission paths used in [2] to evaluate generic clock recovery loop behavior as a function of transmission path. Transmission path lengths were 4", 16" and 24". The data rate was 5.0 Gb/s and the injected RJ was 0.05UI with uniform spectral density from 0 Hz to 2.5 GHz. The simulations for this study were run for 10^8 bits.

Figure 1 is a graph of the magnitude of the jitter transfer function for each of the three path lengths. In this Figure, the 3dB bandwidth of the clock recovery loop decreases from 12.1 MHz for the 4" path to 6.1 MHz for the 24" path. Figure 1 also shows a rational transfer function fit to the 4" path jitter transfer function. The poles are at -14 MHz and -33 MHz.

Figure 1. Jitter transfer function magnitude as a function of frequency and transmission path length

Figure 2 is a polar plot of the jitter transfer functions. Note that although the clock recovery loop bandwidth varies as a function of transmission path length, the polar plot of the jitter transfer function remains the same. This characteristic was observed for every SerDes design studied for this paper. Each clock recovery loop has a phase detector that somehow compares the data transition times to the clock edges. One possible explanation for the invariance of the polar shape is that intersymbol interference reduces the sensitivity of this phase detection mechanism, and the reduced phase detector sensitivity reduces the clock recovery loop bandwidth

Figure 3 is plot of the magnitude of the pattern dependent jitter as a function of frequency. It appears that, at least at low frequencies, the pattern dependent jitter is a uniformly distributed Gaussian process that is then filtered by the clock recovery loop. Note that as the transmission path gets longer, the pattern dependent jitter at low frequencies increases as the loop bandwidth decreases. The net result is that the pattern dependent jitter remains nearly constant. For the case studied, the pattern dependent jitter was 0.83 ps rms for the 4" path, 0.87 ps rms for the 16" path, and 0.98 ps rms for the 24" path. We examined the correlation between deterministic jitter (DJ) and pattern dependent jitter and concluded that although there was a weak correlation, DJ does not seem to be a sensitive predictor of pattern dependent jitter.



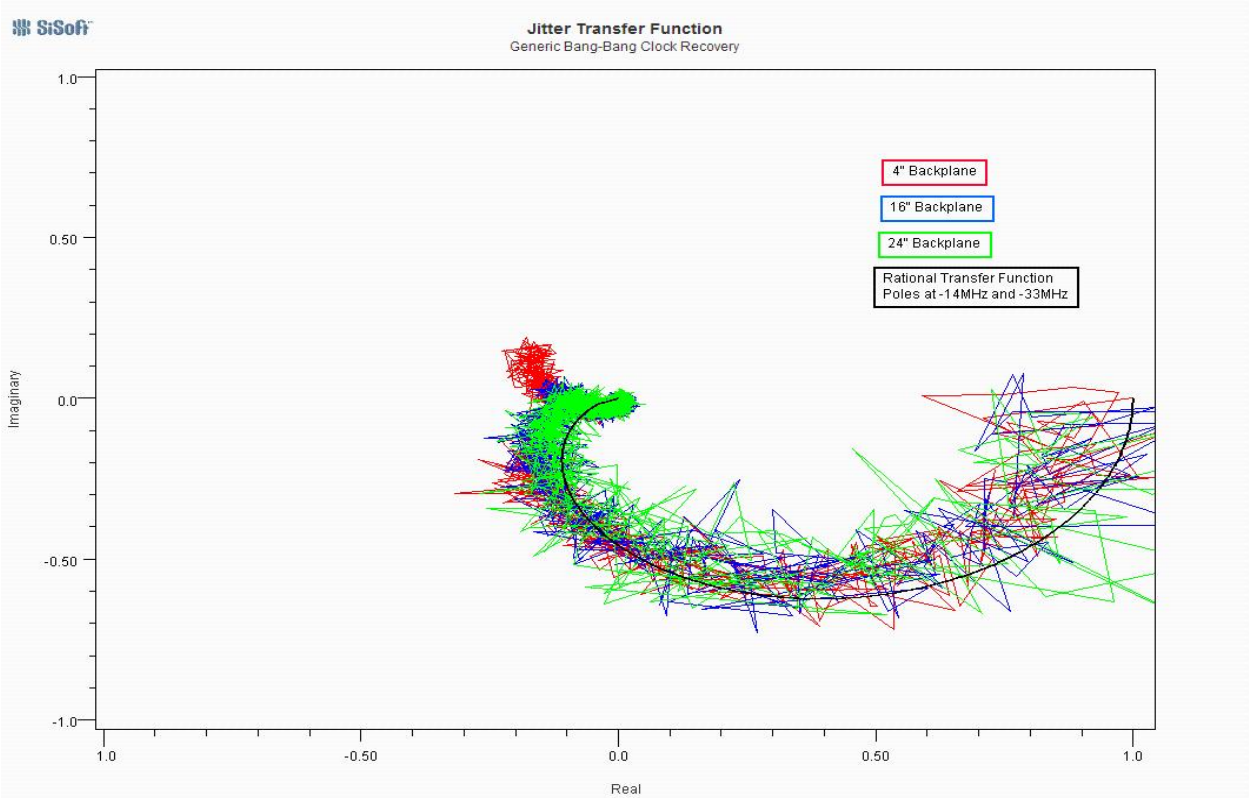
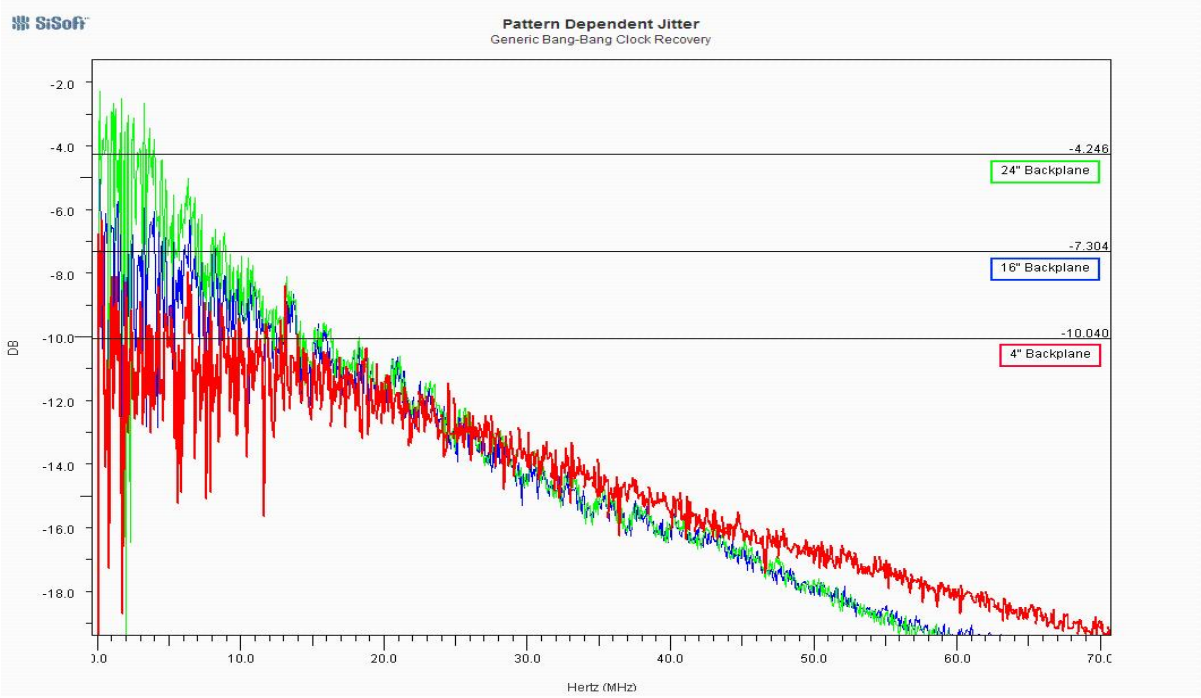


Figure 2. transfer functions

Polar plot of jitter



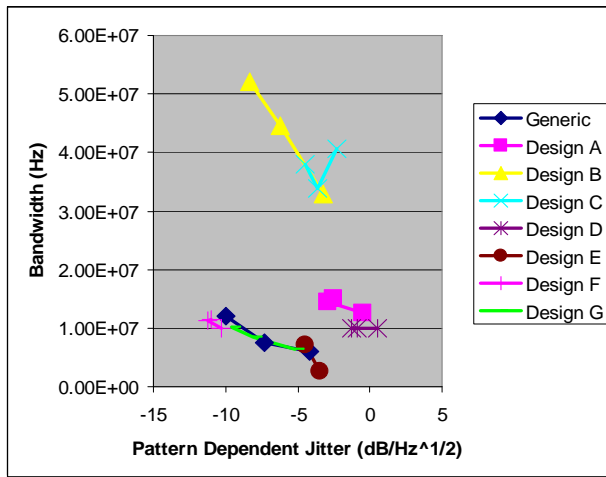


Figure 4. Jitter transfer function bandwidth vs. pattern dependent jitter spectral density for seven different SerDes designs and three different transmission paths

The method described above was applied to seven different IBIS-AMI models from six different IP vendors. Figure 4 is a plot of the clock recovery loop bandwidth vs. pattern dependent jitter for each of these designs and for all three transmission paths.

In general, higher loop bandwidth is desirable because the clock recovery loop will do a better job of tracking out phase noise from the reference clock or the transmitter. A low spectral density of pattern dependent jitter is also desirable, although pattern dependent jitter is typically much lower than other sources of phase noise such as phase noise due to power supply noise. Thus, the upper left corner of Figure 4 is the most desirable.

From Figure 4, it is clear that there is considerable variation in clock recovery performance, with jitter transfer function bandwidth varying from 1.5 MHz to 50 MHz and pattern dependent jitter spectral density varying from -11 to $+0.5 \text{ dB} / \sqrt{\text{Hz}}$ for exactly the same conditions.

IV. CONCLUSIONS

This paper has demonstrated the use of IBIS-AMI models to study the clock recovery loop behavior of seven different SerDes designs from six different IP vendors. The conclusions of this analysis are

1. Clock recovery loop performance varies significantly between SerDes designs.
2. Total pattern dependent jitter remains nearly constant as a function of transmission path.
3. The polar shape of the jitter transfer function remains constant as a function of transmission path even though the transfer function bandwidth varies significantly.

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