ASSESSING AND IMPROVING THE QUALITY OF IBIS MODELS

Kevin M. Fisher
Barry S. Katz
Robert G. H. Moles
Dr. Walter M. Katz
John Figueroa, P.E.

Signal Integrity Software Inc.
www.sisoft.com

Apple Computer
www.apple.com

Abstract

Despite the advantages of using IBIS models for the design of high-speed systems, many users report that models produce incorrect results and lack portability. The set of typical experiences indicates that the industry's process for assuring good IBIS models is in need of redirection. Progress has been made in the area of checking syntax and basic data correctness. However, standard methods do not exist to measure the capabilities and limitations of a model supporting high-speed integrated signal integrity and timing analysis in a system verification environment. Offered here is a quality rating system for IBIS models; demonstrating compelling results with improvements to models from multiple semiconductor vendors.

Authors Biographies

Kevin Fisher is an SI Consultant at Signal Integrity Software. While at Digital Equipment Corporation, Mr. Fisher developed tools to automate the signal integrity process in the areas of solution space analysis, waveform extraction, SPICE deck generation, and timing analysis. Currently, he has been the technical lead on the development of an IBIS model certification process, and is developing tools to automate the validation of engineering model libraries, as well as consulting on the SI and timing analysis to SiSoft customers. He received a BSCE from the University of Cincinnati.

Barry Katz has been at the forefront of high-speed design throughout his career, devoting his efforts to solving the problems faced by designers of leading edge high-speed systems. In 1995, Mr. Katz founded Signal Integrity Software, Inc. (SiSoft). He has assembled a team of world-class experts committed to solving the industry's most challenging high-speed design problems by delivering a comprehensive design methodology, software tools, and expert consulting.

Mr. Katz has been a major influence on the signal integrity methodology utilized by numerous companies and has led multiple signal integrity design teams. He has expertise in all aspects of high-speed design including: timing analysis, interconnect analysis, crosstalk analysis, electromagnetic modeling of interconnect, packages and connectors, I/O buffer analysis and selection, decoupling analysis, simultaneously switching output analysis, interconnect topology, termination selection, clock distribution and skew analysis, and high-speed bus design.

Mr. Katz has developed software products for timing-driven crosstalk analysis and timing-driven hierarchical floor planning as well as consulted for multiple EDA vendors on the underlying functionality and algorithms of their signal integrity tool suites. At Digital Equipment Corporation he developed signal integrity tools for PCB extraction, crosstalk analysis, and interconnect simulation and was Digital's first representative to the IBIS consortium. Mr. Katz holds a MSEE from Carnegie Mellon and a BSEE from the University of Florida.

Robert Moles has worked with board designers in the computer industry on all aspects of signal integrity ranging from the chip IO cell at the transistor level through package, pc board, backplane to cable interfaces, as well as board stackup design and layout rules, optimization of terminations, and modeling of packages, boards and connectors and their simulation in SPICE. At Honeywell-Bull until 1991 he provided technical leadership in SPICE modeling, interconnection technology, clock systems and timing analysis at VLSI chip, board, backplane and system interface design levels for midframes and minicomputers. He obtained compliance with "Corporation for Open Systems" 802.3 (Ethernet) LAN conformance tests, resulting in the company being the first to receive the COS Mark for 802.3 internetworking. At Data General, he analyzed difficult signal integrity problems involving ECLinPS speed and other technologies for a high-end minicomputer, long etch and cable expansion PCI buses for servers, as well as 500 Mbyte/s (4ns) SCI cable interfaces for NUMA using LVDS. More recently he has consulted with Compaq on DDR SRAM, 500 Mt/s system bus, package noise, clock distribution and PLL jitter sources, optimizing PCI driver characteristics. Mr. Moles has four patents in computers and data communications. He has a BS (Eng) from London University, England, and has completed selected graduate courses at Toronto, McMaster and Northeastern Universities.

Dr. Walter Katz is a pioneer in the development of constraint-driven printed circuit board routers. He developed SciCards, the first commercially successful autorouter. Dr. Katz founded Layout Concepts and sold routers through Cadence, Zuken, Daisix, Intergraph and Accel. More than 20,000 of his tools have been used worldwide.

Dr. Katz developed the first signal integrity tools for a 17 MHz 32-bit minicomputer in the seventies. In 1991, IBM used his software to design a 1 GHz computer.

Dr. Katz holds a PhD from University of Rochester and a BS from Polytechnic Institute of Brooklyn.

John Figueroa is the ECAD manager for all hardware products at Apple computer in Cupertino California. He is responsible for tools, processes and next generation methodologies associated with board level design and simulation. Mr. Figueroa has been involved in electronic systems design and test since 1974. He holds a BSEE and has done graduate work at Stanford University in signal processing. He has authored papers for the Microprocessor report and IEEE Compcom, and written bus design software performing timing analysis. He developed rapid design methodologies for C-Cube for shipment of millions of low cost DVD, VCD players in the China marketplace, sensitive to EMC in a low-cost manufacturing environment. He has delivered seminars on rapid design methods and “EMC-Lite”™ seminars. Mr. Figueroa is an IEEE member, former IEEE chair, university mentor, and former director of the Silicon Valley Engineering Council.

The Current State of IBIS Models

The I/O Buffer Information Specification was first introduced by Intel Corporation to allow the dissemination of behavioral characteristics of I/O buffer circuitry from semiconductor vendors to EDA application development groups and computer system designers.

Since its inauguration, IBIS models have gained wide acceptance by vendors, software developers, and end-users alike. The IBIS standard allows semiconductor vendors to give their end-users a 'black box' electrical model to use in their circuit simulations without distributing proprietary transistor level information. The EDA industry was quick to provide support for IBIS either by directly reading IBIS into their simulator engines, or by translating the IBIS models into formats compatible with their products. End-users embraced the IBIS standard because its standardized format provides a 'plug in' capability for the IBIS component, it can encapsulate a large amount of signal integrity information, and IBIS models are much faster to simulate with than SPICE models.

In 1993 the IBIS Open Forum was created to drive the development of this standard. As the acceptance of the standard increased, so did the effort of the Forum and the IBIS community. These efforts were designed to keep the IBIS specification current with SI issues, provide tools to create, assess, and edit the data contained in the models, and to educate the industry on the proper creation of these models.

To date, contributions made by the IBIS Open Forum IBIS community include, but are not limited to:

- **IBISchk (Golden Parser)** – software parser developed and supported by the Forum to check IBIS files for proper syntax and the existence of basic waveform levels, such as the existence of Vinl and Vinh for Input models. IBISchk also has some more advanced features, such as load-line calculation of Output and IO models with the AC test loads to determine whether the model will drive through the measure point Vmeas and to identify inconsistencies between IV and VT curves.
- **Spice2IBIS** - software developed and maintained by North Carolina State University to generate IBIS data curves from SPICE models and to merge SI/Timing information with the results.
- **Visual IBIS Editor** – Software provided by Innoveda/HyperLynx to view behavioral data curves and edit model information.
- **The IBIS Cookbook** - a tutorial on how to create IBIS models from source data, whether it is from SPICE models or from lab measurements of the physical component.
- **The IBIS Accuracy Specification** – documentation on how to correlate IBIS model data with the physical component, and a template to report the results.
- **Model review service for IC manufacturers** offered by the Forum.

The above software tools and documentation are very useful and very thorough in areas such as IBIS component development, curve data accuracy assessment, and syntax and basic data correctness. Yet the quality of IBIS models used in the industry today varies tremendously, but is generally poor.

IBIS Models Not Passing Golden Parser

We ran commonly used IBIS components from ten major semiconductor vendors through the IBISchk3 Golden Parser and show the results in Fig 1. Out of the 52 components tested, 17 of these failed the Golden Parser, with failures coming from components supplied by four of the vendors. One of the components supplied from a very prominent semiconductor vendor had 46 errors! One can only assume

that no checking was done on any of the data in these models since they could not be processed by any simulator supporting IBIS.

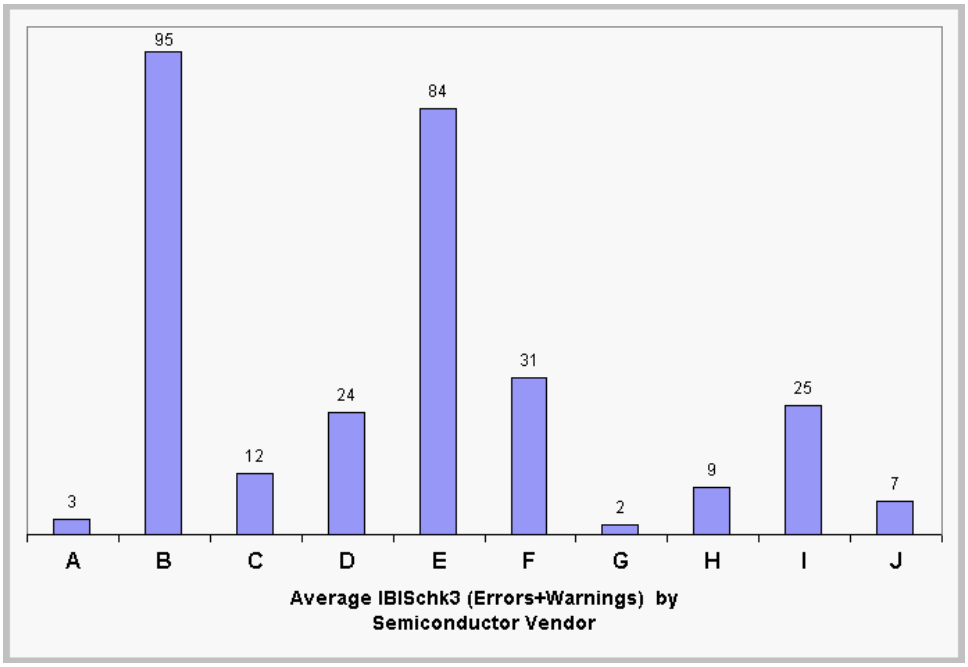

Figure 1: Average Total IBISchk3 Errors and Warnings by Vendor

Common Mistakes Leading to Incorrect Results

In addition to the syntax errors and warnings caught by the Golden Parser, there are also common mistakes made in the industry, whether they are in the development of the component, or in the use of the component, that can lead to incorrect results when used in simulation. These common mistakes are detailed below.

Common Mistake #1: Improper Translation of I-V Data Curves

After obtaining raw I-V data for an IBIS model, one step in the development process is the translation (or shifting and rotating) of the [Pullup] and [Power Clamp] curves for Output or I/O cells, and of the [Power Clamp] curves for Input cells. This translation is done to set the voltage in the curves relative to Vcc instead of relative to ground. Figure 2 shows a graph of the [Pullup] curves over process of a model not properly translated and Figure 3 shows what these [Pullup] curves should look like after Vcc translation:

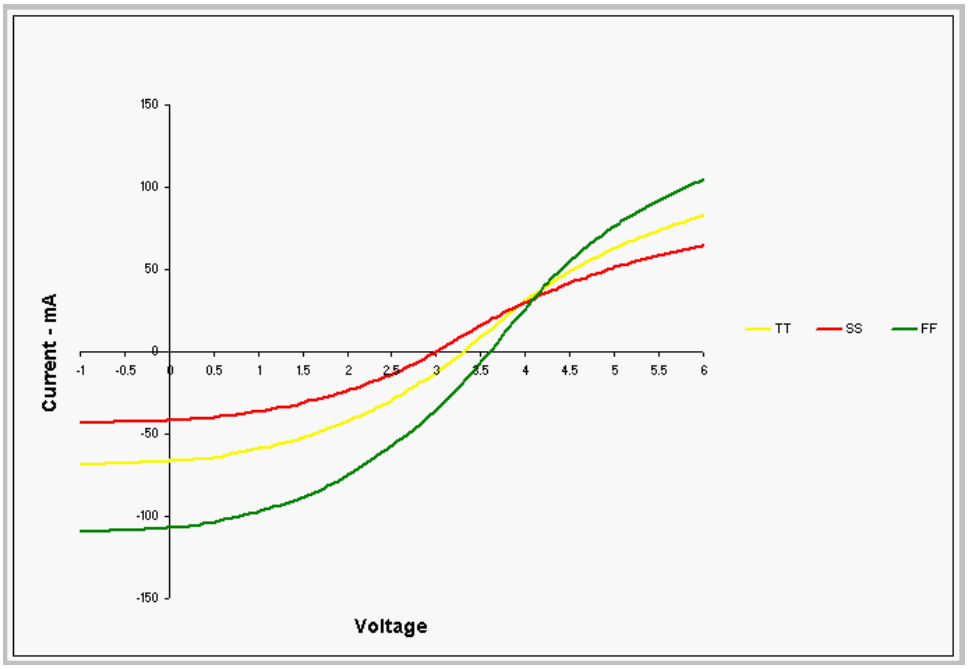

Figure 2: Raw Non-Translated Pullup IV Curves by Process

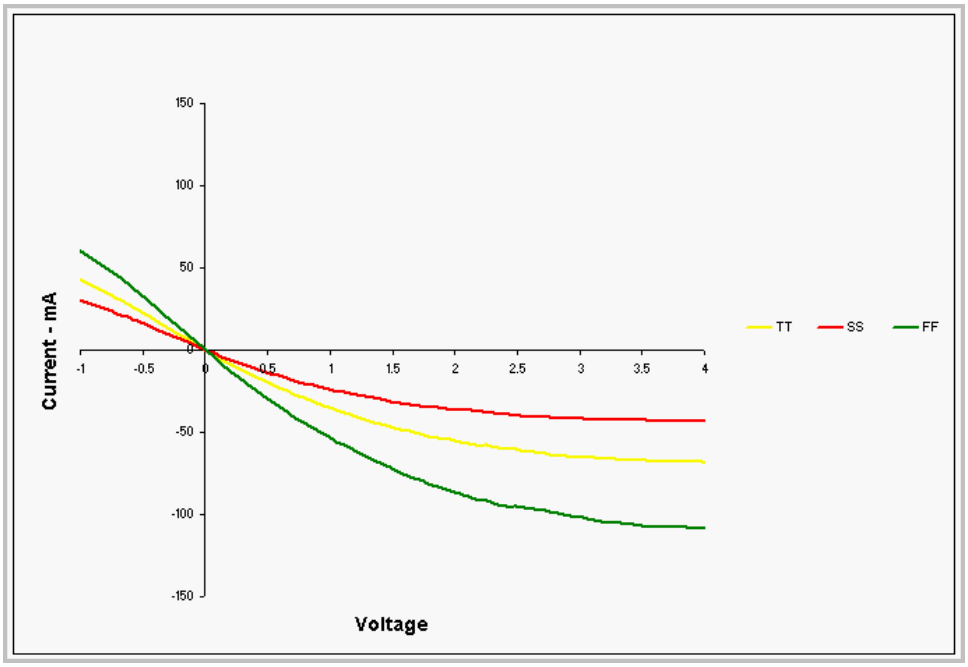

Figure 3: Translated (IBIS) Pullup IV Curves by Process

Common Mistake #2: Improper Subtraction of Clamp Diode Current in I-V Data Curves

Another step in the development process of I/O cells is the separation, or subtraction, of the clamping diode current from the current flowing in the driver itself. This step is necessary for I/O cells, as the simulator will automatically superimpose the clamping diode current on the transistor drive current when the cell is acting as a driver. Failure to subtract the clamping data from the device drive data will cause the simulator to "double-count" the clamp diode data, giving an incorrect modeling of the clamps.

Figures 4 and 5 show the set of [Pulldown] IV curves over process with and without subtraction of the clamping characteristics.

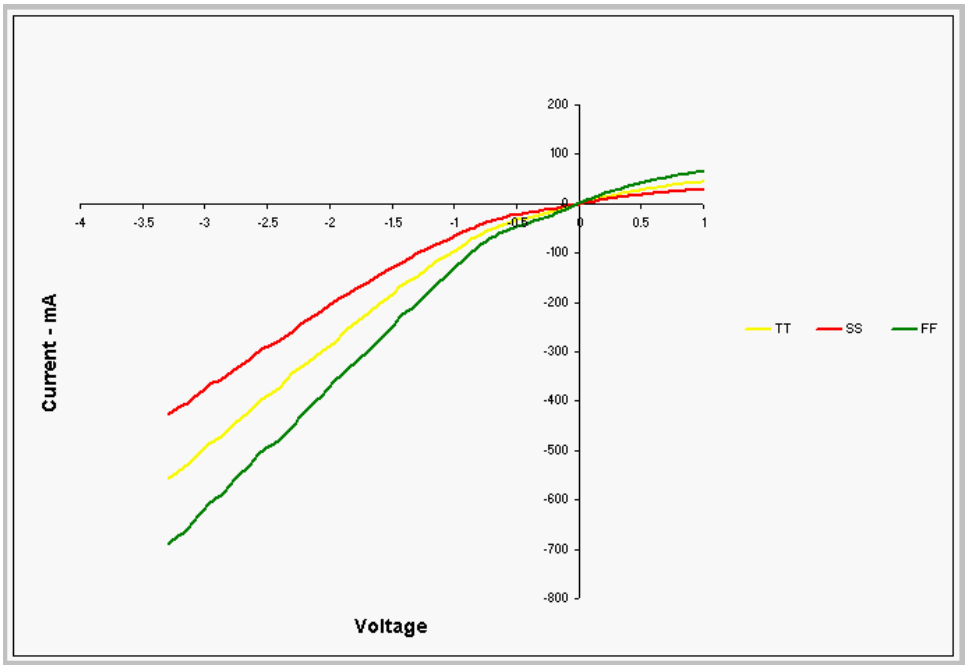

Figure 4: Pull-Down IV curve without clamps subtracted

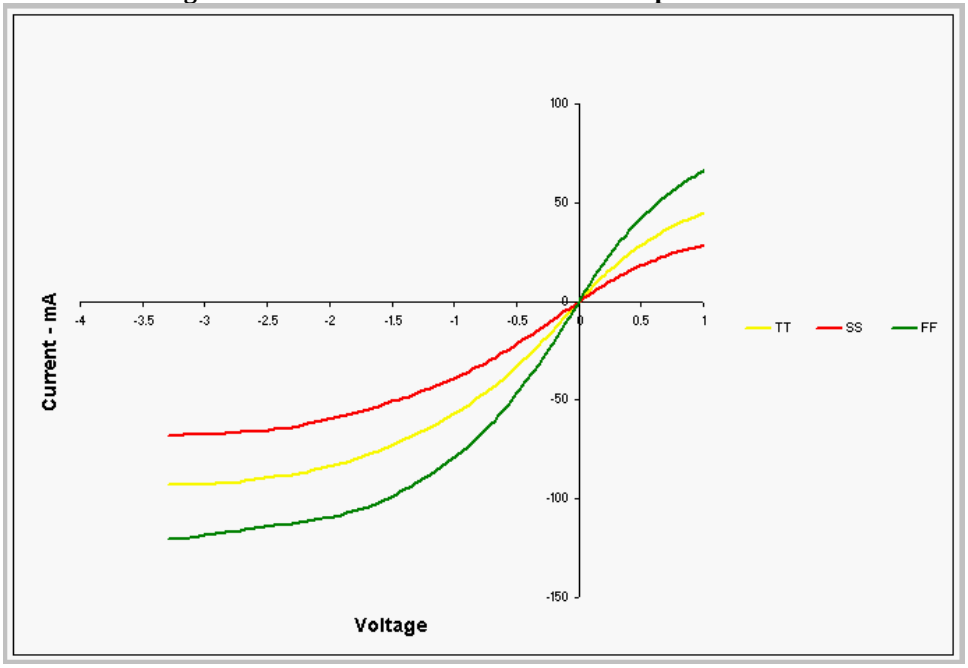

Figure 5: Pull-Down IV curve with clamps subtracted

Common Mistake #3: Improper Usage of Device Power Supply

The [Voltage Range] parameter in an IBIS model specifies the power level at which the model is to be supplied with when used in simulation. This value may or may not correspond, however, to the power level at which the model's curve and ramp data was generated. Contrary to popular belief, the drive

characteristics of the model are locked at creation time, and cannot be changed simply by changing the [Voltage Range] parameter in the IBIS file. Figure 6 illustrates the differences in [Pullup] and [Pulldown] drive strength of an SSTL I/O model generated by two different power supply levels.

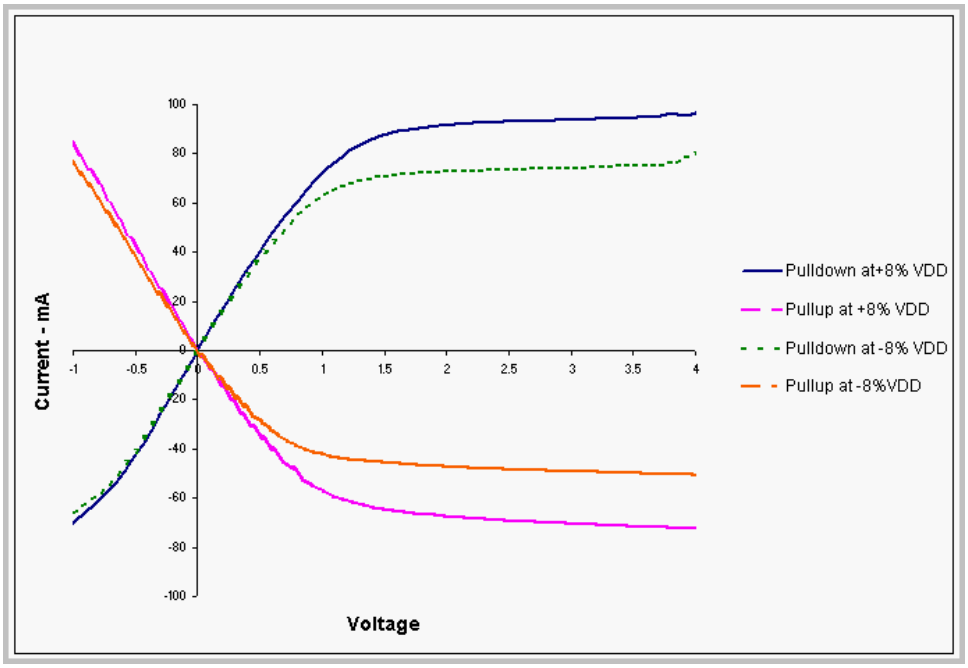

Figure 6: SSTL IBIS Pullup and Pulldown curves generated at two voltage rails

Except for the power supply voltage, all other factors affecting the generation of these curves have been held constant, including: Process Corner (TT) and Temperature. The only cause of the discrepancies in the I-V curves above is the power supply voltage. At 2.0V the SSTL I/O model created with a 2.7V voltage rail has a [Pullup] current of ~ -67mA, while the model created with a 2.3V supply has a [Pullup] current of ~ 47mA, for a difference in drive strength of 20mA (or 42.6%). The [Pulldown] curves give comparable results.

Lack of Signal Integrity Information

Along with common problems encountered in either model creation or model use with the IBIS model data curves, IBIS models are usually missing data required to do proper signal integrity and timing analysis. Generally, SI information included in IBIS models is usually limited to the input threshold parameters 'Vinl' and 'Vinh' (Input and I/O). This gives the end-user only enough information to verify input transitions. No other waveform DRCs (Design Rule Checks) can be performed without the entry of more information. Although most parameters needed for waveform and timing analysis are usually provided on the component datasheet, the retrieval of this information is very tedious and tends to be error-prone. Ideally, the population of this information should be managed by a librarian or best case, should be incorporated as part of a semiconductor vendor's process for IBIS model generation.

The Importance of IBIS Quality

Incorporation of an IBIS quality validation process is vital to guarantee that an IBIS component will produce the correct analysis results, or even any results at all. The use of non-validated IBIS components in high-speed system design analysis and verification compromises the integrity of the simulations, analysis, and ultimately, the final product, potentially causing some or all of the following:

- Design instability
- Product failure
- Multiple re-spins
- Increased time-to-market
- Product recall

Bottom Line: A well-defined, well-documented quality validation process for IBIS components is needed in high-speed system designs to ensure the product success.

An Approach to Assessing and Improving IBIS Quality

The Challenges of Supplying a High-Quality IBIS Model: What is bad, what is good?

Verifying that an IBIS component meets the needs of every engineer in the industry is a non-trivial task. Some issues that impede validating an IBIS component for all cases are:

- System design and verification projects do not all have the same scope, affecting the requirements of the model
- Vendor software tools have inconsistent levels of IBIS feature support
- Some problems found in a validation process can be fixed by the user, while others cannot
- It is difficult to determine when transistor level models are required because of IBIS limitations, simulator limitations, or the way the IBIS models were created

In order for an IBIS quality validation process to be successful, the process should be able to: identify general problems with IBIS syntax, address common mistakes made throughout the industry; and identify data requirements to be met. A successful process should also be adaptable to multiple projects that may have varying analysis scope and environment. SiQ™, an approach to IBIS component quality validation, has been developed that addresses these issues.

The SiQ IBIS Component Quality Validation Process: An Overview

The SiQ quality validation process centers on the application. When end-users validate models for use in high-speed system design analysis, the component should be qualified for maximum functionality, but not all the results may be relevant. The end-user should only be concerned with the qualification of the component for uses applicable to the analysis scope of their project.

The assessment of the quality of an IBIS component can be broken into five categories:

- Fundamental Model Behavioral Accuracy and Completeness
- SI/Waveform Analysis
- Timing Analysis
- System-Level/Post-Layout Verification
- Simulation Model Portability

The high level categories listed above can be further broken down into sets of functionalities. Each of these functionalities has a set of IBIS data parameters associated with it, and a particular use in high-speed system design analysis.

When qualifying an IBIS component for a given set of functionality, we are only concerned with the data relevant to that functionality. We look at the individual IBIS data parameters associated with the functionality and the data values tied to the parameters, and ask the following questions:

- Is the data parameter syntactically correct (i.e. unit syntax)?
- Is the data parameter defined in the component (i.e. unit completeness)?
- Is the value in the data parameter correct (i.e. unit correctness)?

The issue of unit syntax is trivial, and can be checked for all data parameters in an IBIS component by running the IBISchk3 Golden Parser, as described previously. The process of verifying unit completeness is also straightforward, and can be done using a software parser to check for the existence of all data parameters in an IBIS component. Checking data parameters for correctness is not easy, however. Each parameter needs to be checked individually, and is usually a manual process of checking against values defined in the component's datasheet, data extracted from SPICE simulation, and lab measurements.

When issues arise with a data parameter, incomplete, incorrect, or syntax related, a way is needed to fix these issues. Some data in an IBIS file can be fixed with the simple changing of a value, or by simple edits to the file to correct syntax. Some data, however, can only be fixed by data regeneration through SPICE simulation or lab measurement and is often only producible by the semiconductor vendor.

Given that an engineer may only be concerned with the qualification of the component for uses applicable to their project, whoever is responsible for validating the model should also include a report showing the capabilities and limitations of the model in a standard, easy to read format so that the engineer can quickly ascertain whether this model will meet the need of the specific project.

Fundamental Model Behavioral Accuracy and Completeness

The data in this category includes all information that will affect the resulting waveforms in the target simulator. The following data must be checked for each model:

- Existence
- IV curves
- VT curves
- Ramp
- Component capacitance

- Package models

There are two levels of checking here. One is a high-level "sanity" check and can be done automatically. For example, checks can be performed to determine if each of the IV curves exist, is in the correct quadrant, and if there are inconsistencies between the IV and VT curves. Data with non-realistic or missing values are identified. A more detailed assessment of the model can be performed if SPICE netlists, extracted lab measurements, or detailed package information is available.

SI/Waveform Analysis

IBIS version 3.2 supports up to thirteen voltage levels (Figure 7) and two time durations under which waveform analysis can be performed. Proper assignment of these parameters allows signal integrity tools to extract waveform violations for static overshoot, dynamic overshoot, static ring-back and dynamic ring-back. Many of these parameters are optional, but without definition, application of an IBIS model can be somewhat limited.

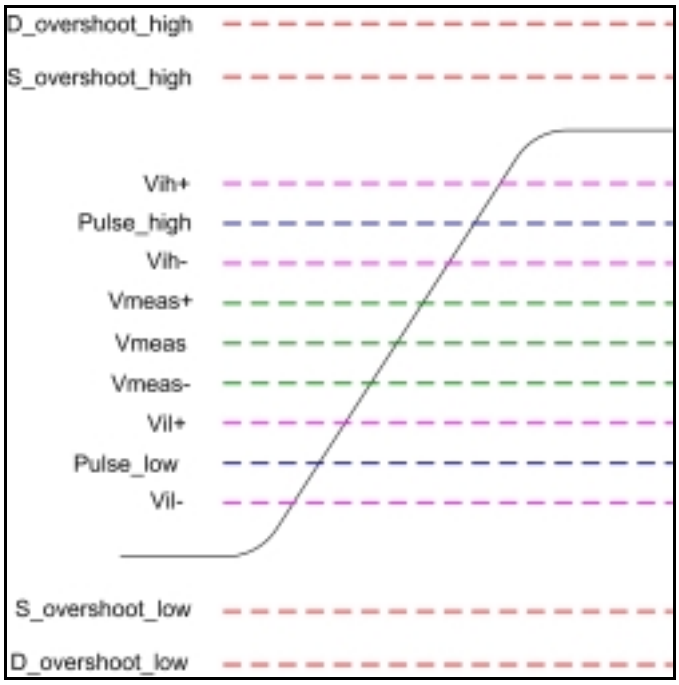

Figure 7: IBIS Waveform Analysis Voltage Levels

Timing Analysis

The key to performing timing analysis is to properly define the standard load and the Vih/Vil/Vmeas levels for waveform measurement. The importance of the standard load is commonly misunderstood. Standard loads serve as a point of reference for both the semiconductor vendors and the end-users of an IC. Semiconductor vendors ensure their chips meet their timing specifications with the standard load. End-users then measure interconnect timing from one IC to another relative to this same point of reference, so that when the interconnect delays are added to the delay of the IC during static timing analysis, delays are properly accounted for.

System-Level/Post-Layout Verification

System level verification is important when performing high-speed system design. Not only should engineers perform upfront pre-layout analysis to generate layout rules that satisfy waveform and timing constraints, but they should also verify that the actual system implementation satisfies the waveform and timing constraints as well. In order to do this, it is critical that the physical pin numbers map to the CAD database and that the logical pin names map to other library elements. It is also important to ensure that the proper models are assigned to each pin and proper model type is assigned to each model.

Simulation Model Portability

There are a lot of subtleties to consider when an IBIS model is used with a variety of signal integrity tools. Some tools are more lenient than others and actually correct some of the common mistakes prevalent in IBIS models. Different tools have different levels of capability when it comes to waveform processing and timing analysis. For instance, they may not be able to utilize the thirteen voltage levels in Figure 7 even if they were all defined in an IBIS model.

Results - The "True Capabilities" of IBIS Models Using the SiQ Approach

Using the SiQ approach, the same 52 IBIS components from 10 semiconductor vendors mentioned at the beginning of this paper were analyzed. Figure 8 compares the original models to the same models after being corrected using the SiQ validation process while using IBISchk3 errors and warnings as a figure of merit.

All of the corrected models scored perfectly. This is good, but not representative of the data the user needs. These models were further enhanced to support more precise timing rules, as well as overshoot and ringback rules. A side-by-side comparison using the SiQ scoring system is provided in Figure 9. This system demonstrates how the IBIS components from the ten vendors were improved through a semi-automated process, in addition to assessing the quality of the IBIS model as targeted for our specific task. Utilizing this approach, multiple systems using IBIS models with speeds exceeding 500MHz were designed, and in most cases the same accuracy obtainable using Hspice models. Although the IBIS behavioral models are not as accurate as Hspice models, the factor of 100 performance increase allowed us to sample a significantly larger solution space in pre-layout analysis and exhaustively verify waveform integrity and timing on all signals of interest on numerous large post-layout databases.

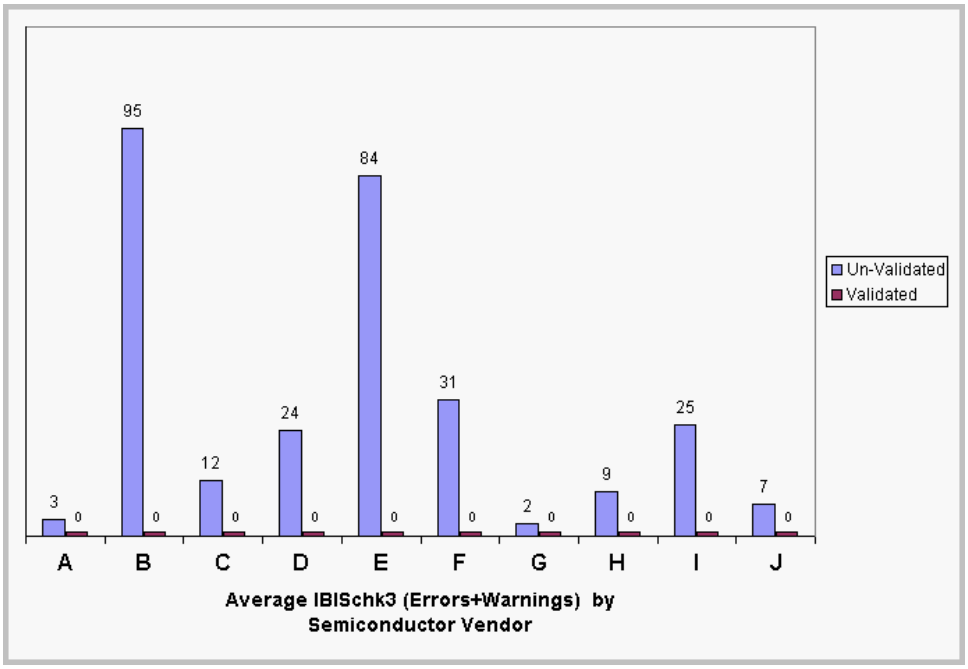

Figure 8: Comparison of Average IBISchk3 Errors and Warnings by Vendor before and after SiQ

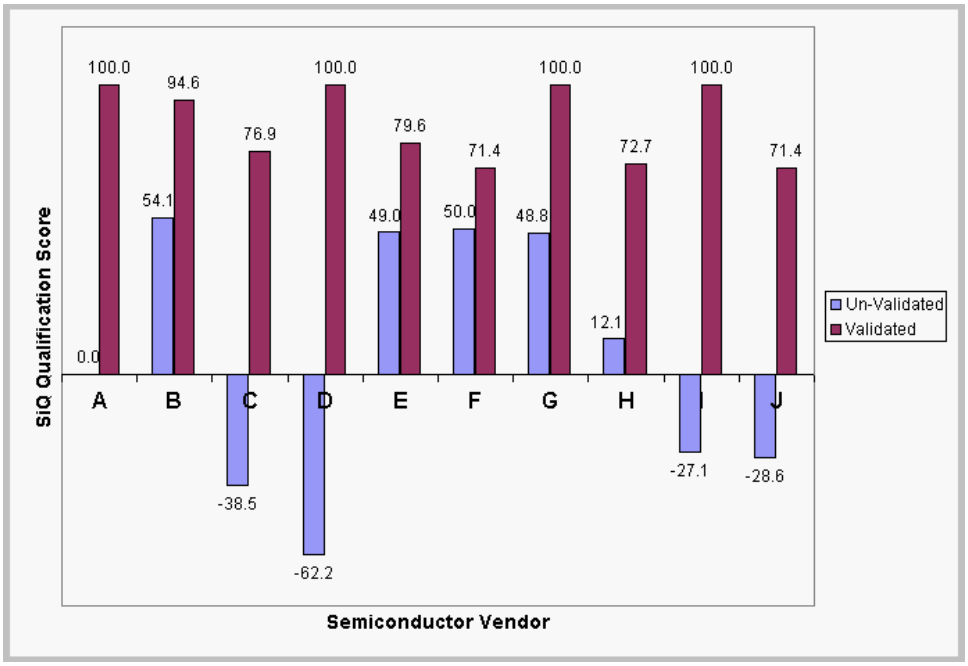

Figure 9: Comparison of SiQ scoring by Vendor before and after improving models

Conclusions

Currently, many IBIS models provided by semiconductor vendors are not acceptable for high-speed system design purposes. Most models lack the information necessary to perform detailed signal integrity and timing analysis. Some models are so bad that they won't run in any simulator or provide meaningless results if they do run. Model users cannot assume any level of quality in these models. However, the current situation is not hopeless. The SiQ quality validation process has identified how poor quality can be, but also how much room for improvement exists. Using the SiQ validation process to qualify IBIS models used in the design of these systems, designers can confidently perform the detailed signal integrity and timing analysis required. Performing this analysis will result in products that get to market faster, at higher performance, with greater stability, and less cost. These benefits have been realized on multiple systems with speeds exceeding 500MHz.

Acknowledgements
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