SOLUTION SPACE ANALYSIS
Attacking the High-Speed Analysis Problem

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"Solution Space Analysis
Attacking The High Speed Analysis Problem"

Abstract

As edge rates and clock frequencies increase, the analysis of high performance networks becomes more difficult. Gone are the days when a best case and worst case set of simulations defined operation. At today's higher frequencies, careful attention must be given to the analysis of skew, etch topology, cross talk, process variations, and packaging. Keeping track of all of these issues is becoming complex, and a way of dealing with all of these issues must be developed. This paper discusses high-speed design concerns and then presents a methodology, Solution Space Analysis, which addresses these concerns. Simply stated, the methodology breaks the analysis into smaller, more manageable components that can be easily understood and modeled. Each of these smaller components is then simulated over a simulation space that may include variations in process, etch length, network topology, environment, and so on. In addition, the methodology describes an approach to handling the affects of Inter-Symbol interference and cross talk. These smaller analysis components lend themselves to automation for the generation of the simulation data and the extraction of the required data. The results from these smaller components can then be re-combined to yield a comprehensive solution that describes the expected design operation.

Authors Biography

Douglas J. Burns graduated Magna cum Laude from the University of Massachusetts in 1981 with his BSEE and received his MSEE from Northeastern University in 1986. Between 1981 and 2000, Doug worked for Honeywell, Digital, and Compaq Computer. He has led VLSI design implementation teams, signal integrity teams, ASIC implementation teams, and influenced the system architecture of ALPHA systems. Doug consulted on SI and implementation issues across many groups within Digital/Compaq, and has a successful track record of bringing products to market. Current, Doug holds four patents in computer system design and has two additional patents pending. Doug's expertise spans a wide range of engineering disciplines including: system architecture, VLSI design, package design, timing analysis, interconnect analysis, cross-talk analysis, electromagnetic modeling, IO buffer analysis and selection, simultaneously switching output analysis, termination selection, clock distribution and skew analysis, and high-speed bus design.

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Stephen R. Coe received his BS in Electrical Engineering from the University of Massachusetts in 1983. Steve began his signal integrity career when he joined Digital Equipment Corporation in 1987. During his 13 years there, he solved the signal integrity issues for many of Digital's high performance computers. Steve influenced the design of many high performance memory, PCI and AGP systems. He has been a major contributor to the signal integrity methodology utilized in the design of VAX and Alpha based workstations and servers. He holds patents on several Alpha server products. More recently, Steve worked on the design of high-speed network appliances including routers, switches and hubs at Nortel Networks. Steve is an expert in the analysis of interconnect, crosstalk and timing, as well as interconnect topology and termination selection, I/O selection, and electromagnetic modeling of interconnect, packages and connectors.

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Dr. Walter Katz is a pioneer in the development of constraint-driven printed circuit board routers. He developed SciCards, the first commercially successful autorouter. Dr. Katz founded Layout Concepts and sold routers through Cadence, Zuken, Daisix, Intergraph and Accel. More than 20,000 of his tools have been used worldwide.

Dr. Katz developed the first signal integrity tools for a 17 MHz 32-bit minicomputer in the seventies. In 1991, IBM used his software to design a 1 GHz computer.

Dr. Katz holds a PhD from University of Rochester and a BS from Polytechnic Institute of Brooklyn.

Barry Katz has been at the forefront of high-speed design throughout his career, devoting his efforts to solving the problems faced by designers of leading edge high-speed systems. In 1995, Mr. Katz founded Signal Integrity Software, Inc. (SiSoft). He has assembled a team of world-class experts committed to solving the industry's most challenging high-speed design problems by delivering a comprehensive design methodology, software tools, and expert consulting.

Mr. Katz has been a major influence on the signal integrity methodology utilized by numerous companies and has led multiple signal integrity design teams. He has expertise in all aspects of high-speed design including: timing analysis, interconnect analysis, crosstalk analysis, electromagnetic modeling of interconnect, packages and connectors, I/O buffer analysis and selection, decoupling analysis, simultaneously switching output analysis, interconnect topology, termination selection, clock distribution and skew analysis, and high-speed bus design.

Mr. Katz has developed software products for timing-driven crosstalk analysis and timing-driven hierarchical floor planning as well as consulted for multiple EDA vendors on the underlying functionality and algorithms of their signal integrity tool suites. At Digital Equipment Corporation he developed signal integrity tools for PCB extraction, crosstalk analysis, and interconnect simulation and was Digital's first representative to the IBIS consortium. Mr. Katz holds a MSEE from Carnegie Mellon and a BSEE from the University of Florida.

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Introduction

Design Partitioning

To properly analyze inter-chip communication, the networks between chips need to be broken down into specific cases of a single source and one or more loads. We define these cases as transfer classes because each case defines a potential transfer from one device to another. In addition, an understanding of the allowable modes of operation for each chip is needed. This means that the designer needs to identify which buses are unidirectional, bi-directional, bus turn around conditions, etc. With the transfer classes defined, criteria for acceptable operating limits must be specified. These limits are generally defined as the overshoot, undershoot, Vol, Voh, and operating frequency.

Timing Requirements

The timing of all networks can be broken down into four basic components:

- Output delay of the source device
- Interconnect delay between the source and destination
- Skew between the source and target clock systems
- Target setup and hold requirements

As part of the design setup, the output delay characteristics of a device need to be identified. These characteristics include both the minimum and maximum delays over the expected operational range and are provided in the device AC specifications. All devices that receive data have a setup and hold requirement. The setup requirement defines the minimum time that data must arrive at the pins of a device before the targeted clock edge. The hold requirement defines the minimum time that data must be held after the targeted clock edge. Once a clock system has been defined, the Clock skew between the source and target device can be determined. With output delay, setup/hold requirements and the clock skew, the ranges of allowable interconnect delays can be computed for the network.

Factors Affecting Timing

In the ideal world, output delay (Clk2out), Setup time, Hold time, and Interconnect delay are accurately known. Unfortunately there are a number of factors that put uncertainty into the numbers and a detailed analysis is required to understand their effects. These factors include:

- Clock Skew: Variation in time that the synchronous clock arrives at the source and destination devices. For setup timing, Setup_Clock_Skew has the effect of having the source device driving later in the clock cycle. This results in reduced setup margin. For hold timing, Hold_Clock_Skew can make the destination clock occur later. This results in reduced hold margin. Minimization of Setup_Clock_Skew and Hold_Clock_Skew requires eliminating differences in the clock path between the source and target devices. Techniques to minimize these skews include:
  - Using a radial clock distribution
  - Matching clock etch lengths (total length and length on any routing layer)
  - Matching Via counts
  - Proper use of Phase Locked Loops (PLL) (both on die and system level)
  - Utilization of high fanout buffers to reduce component variations
- IC Process: Due to variations that occur during IC processing, transistors and on-die etch have ranges of operation. IC foundries guarantee that parts they deliver will operate with a specific range of performance based upon the IC process characteristics, thermal environment, and applied voltage. They supply data describing the AC specs and IO buffer characteristics for fast (FF), typical (TT), and slow (SS) process parts. These characteristics bound the expected operating region.
- Simultaneous Switched Outputs (SSO): Output delay characteristics of IC chips can vary depending upon the number of outputs switching. This is due to voltage variations on the chip and coupling within the package.

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- Interconnect: Bussed signals can be routed on different layers and may have minor topology differences that induce variations in how the signals propagate. In addition, variations in the dielectric and conductor mechanical features also introduce variations. These interconnect variations include:
  - Number of Via's in a network
  - Via position with a net
  - Length mismatch between signals
  - Etch topology mismatches
  - Etch impedance variation and velocity of propagation variations of +/- 10% between routing layers.
- Inter Symbol Interference (ISI): Traditional timing analysis assumes that signals are quiescent before another transition occurs. As the operating frequencies increase, the likelihood that a line has not settled increases. The effect on one transition from the residual ringing on the line from one or more previous transition results in delay variations. These delay variations are called ISI effects.
- Crosstalk: Noise generated on a net from transitions on nearby interconnects in the circuit board, packages, and connectors. Crosstalk can change the level of the signal on a net and therefore cause variations in the interconnect delay. There are two types of crosstalk to consider:
  - Synchronous Crosstalk: This is crosstalk that occurs between signals that have similar clocking and drive characteristics. An example of this would be signals that make up a bus.
  - Asynchronous Crosstalk: This is crosstalk between two independent signals. An example of this would be two independent buses driven by different clock sources. If the clock sources are truly asynchronous to each other, the crosstalk noise could happen on either bus at any time.

All of the above effects can independently modify the system timing margins. To accurately determine the operating region for a system design, detailed simulation work needs to be done that addresses the affects of the above phenomenon. The process of determining if a specific performance goal can be met is called Solution Space Analysis.

Signal Quality

Good signaling is more than just meeting timing budgets. Good signaling requires that the signals do not exceed the reliability limits of the silicon devices and that the signaling environment provides sufficient noise margin to prevent a false signal from propagating. A robust methodology must check the signals at both the source and loads for different sets of conditions:

- At the Source driver, Undershoot and Overshoot voltages must be observed to insure voltage limits at the driver are not exceeded. This check insures that device reliability is not compromised.
- At active loads (loads receiving data) of a transfer class, checks for Undershoot, Overshoot, Slew rate, Vil, Vih, Monotinicity, and Ring-back need to be performed. As with the previous cases, the Undershoot and Overshoot measurements are done to ensure device reliability. The Vih, Vil, and Ring-back measurements ensure that signals are stable and have adequate noise margins to prevent false signal propagation. All device AC specifications assume a minimum and maximum IO slew-rate. The Slew-rate measurement ensures that the signal transition falls within a region specified by the device. Monotinicity checks ensure that the signal makes a clean transition. This is especially important for clocks since a non-monotonic clock could cause false clocking at a receiver.
- At inactive loads, timing information is unimportant, but Undershoot and Overshoot voltages must be observed to insure voltage limits at the driver are not exceeded. This check insures that device reliability is not compromised. An example would be a transfer between two devices on a bus that logically does not communicate with each other.

Solution Space Methodology

Solution Space Analysis involves the review of all sources of delay variation that can exist in a network, simulation of the network, and the compilation of simulation results to predict system performance. Sources of delay variations are:

- Silicon Process Corner (SS,TT,FF)

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- Environment (Temperature and Voltage)
- Crosstalk
- InterSymbol Interference (ISI)
- Simultaneous Switching Outputs (SSO)
- Interconnect Variations (Topology, etch/impedance variations, terminations)
- Component AC Specs

All of the above components have their own affect on the network delay. With a traditional approach, a matrix of all possible network variables would be created and a set of simulations needed to analyze all of these conditions defined.

The Solution Space Methodology breaks the analysis into a number of smaller simulation groups for each network class. These groups include: Coupled simulations, ISI simulations, SSO simulations, process related simulations, and standard load simulations. These smaller groups result in fewer overall simulations, thus making the full analysis easier. The results from each of these smaller simulation groups are then combined to find the final worst-case network performance.

For clarification, assume the following. If a network contains "N" unique variables that have two distinct modes of operation, then 2^N simulations are needed to simulate all possible conditions. These simulations require fully coupled models and a complex input to ensure proper accounting of coupling, SSO, and ISI affects. Using the Solution Space Methodology presented here, the problem is broken down into smaller components. Crosstalk, SSO, and ISI affects are simulated independently. Removal of the crosstalk and SSO components reduced the number of variables from eight to six. This is a 4x reduction in the number of simulations. Depending upon the network sensitivity to ISI, a greater reduction in the number of simulations may be achieved. In addition, complex models are not needed for the remaining simulations, thus reducing simulation run time.

The solution space for a specific network topology is accomplished by doing multiple simulations using all combinations of the IC (FF an SS process) and etch corners (fast etch, FE, and slow etch, SE). This yields four simulation cases (FFFE, FFSE, SSFE and SSSE) to which various corrections for SSO, crosstalk, and standard load delay are then applied. In CMOS, the FF IC corner simulations use a low temperature and high VDD to yield the fastest possible IC characteristics. The SS IC corner simulations use a high temperature and low VDD to yield the slowest possible IC characteristics. The solution space for the entire network class involves running multiple network topologies to bound the overall network performance.

HSpice is the simulator of choice since HSpice models are supposed to accurately represent the performance of the IO buffers. IBIS models may be used if it can be verified that the IBIS models are sufficiently accurate. If HSpice models are not available, then IBIS models must be relied upon.

With the network simulation classes defined, the input stimulus must be identified. Single edge simulations may not accurately predict network performance under all conditions. A check must be made to determine if ISI could affect the network. To determine the susceptibility of a network to ISI affects, a series of simulations are performed to understand the networks settling time. Figure 1 shows the settling time for four transmission lines with lengths of 2 to 18 inches.

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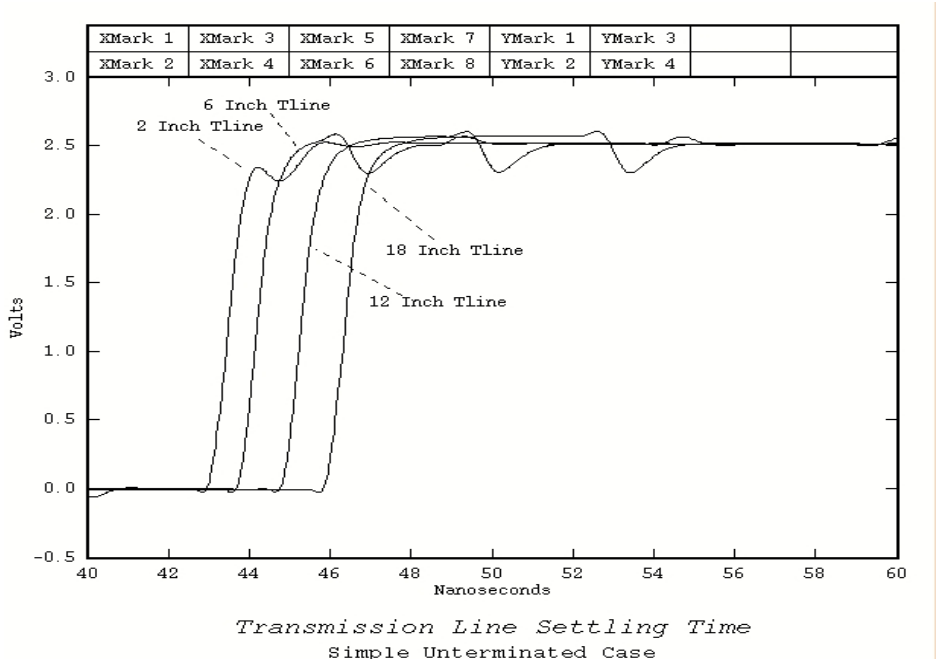
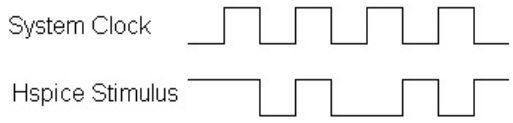
Figure 1



If the data rate is less than network settling time, ISI affects can be ignored. If the ISI affect can not be ignored, then the network needs to be simulated over a range of data rates. To do this a complex piece wise linear waveform can be constructed as the spice file stimulus. The waveform is constructed to generate data transitions that replicate multiple operating frequencies. Figure 2 depicts a representative stimulus waveform used for ISI analysis.

Figure 2



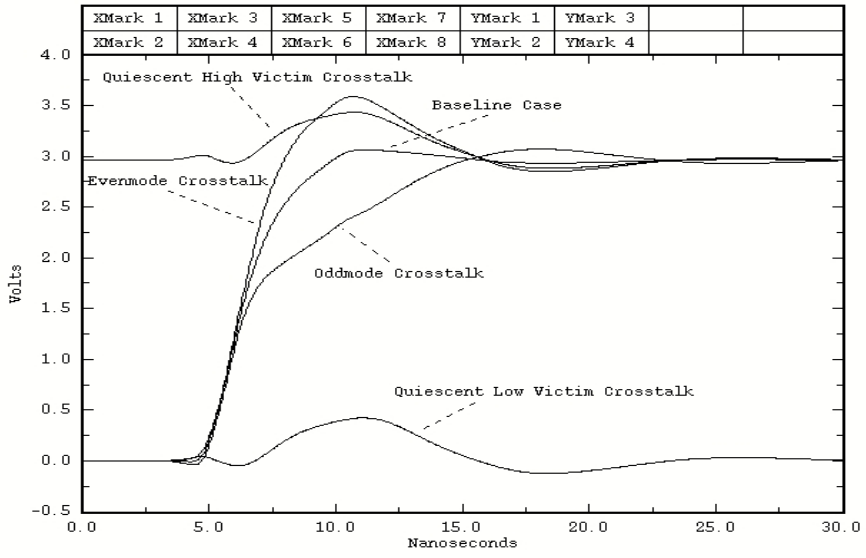
Although crosstalk can be incorporated directly into the simulations, accurate placement of the crosstalk on the victim network is difficult. This is because each network has different aggressors that couple to it in different locations. The goal is not to generate exact models for every network in the system, but to define a crosstalk simulation that bounds crosstalk found in the system. To more accurately determine the effect of crosstalk on interconnect delay, crosstalk simulations are performed with the victim net in both low and high state. The peak value of the crosstalk waveforms on the victim net is then used as a contributor to the waveform noise budget.

SSO can change the voltage level, slew-rate, and delay of an output waveform. Complex coupled spice models are used to see what the effect switching multiple outputs have on a victim net. The results of these simulations can be incorporated into the system timing budget. Vendor specifications may already accounts for the effects of SSO, but these simulations are performed to ensure a full understanding of the package effects on network performance. Five simulation cases are run:

- Baseline Case: Only the victim network is switched. The victim network delays are measured relative to the input stimulus.
- Even Case: The victim and aggressor nodes are switched in phase. Victim network delays are measured relative to the input stimulus.
- Odd Case: The victim and aggressor nodes are switched 180 degrees out of phase. Victim network delays are measured relative to the input stimulus.
- High Case: The Victim is held in the high state and the aggressors are transition high and low. A check is made to ensure that the quiescent signal does not propagate a false value.
- Low Case: The Victim is held in the low state and the aggressors are transition high and low. A check is made to ensure that the quiescent signal does not propagate a false value

Figure 3 shows the simulation affects of the simulation effects of both Crosstalk and SSO.

Figure 3



Crosstalk Simulation, 13" Coupled T-Line Model
4 Aggressors on a Single Victim

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The AC specs of a part are usually specified from pin to pin of a part. It is assumed that the output delays are specified with the output pins driving some standard load. Actual network simulations are done using excitation of the input pin of the driver and delays are measured at the pin of the target load. Since the AC specs of a device already include the IO driver propagation delay, a correction must be made to the network delays by subtracting the delay of the driver driving a standard load. This delay is different for rising and falling edges and for FF and SS IC process corners. The result is the actual network interconnect delay difference from standard load. Since this methodology uses complex stimulus waveforms, each edge of the waveform and the resulting output must be analyzed. These output waveforms must satisfy some basic signal integrity rules including overshoot, undershoot, ring back, monotonicity, slew rate, and proper transition between Vil and Vih. The minimum and maximum interconnect delays are calculated, for each transition, between the time when driver input goes through transition to when the waveform at the load goes through the noise budget adjusted transition voltage. The minimum and maximum of these delays are calculated for all of the rising and falling edges in the simulation, and is further adjusted by the appropriate standard load correction. These results, which represent the interconnect delays for all of the simulations in the solution space, are then collapsed to a single set of rising and falling values (Rmin, Rmax, Fmin, Fmax).

Setup and Hold Margin Calculations

To determine the setup and hold margins for each transfer class, the interconnect delays from the Solution Space Analysis, the clock skew from the clock skew analysis, and the AC spec's of the components involved in the transfer are used as defined in the following equations:

Setup_Margin = Cycle_Time - Max_Clk2out - Max_Etch - Setup_Time -Setup_Clock_Skew

Hold_Margin = Min_Clk2Out + Min_Etch - Hold_Time – Hold_Clock_Skew

Forcing the Setup_Margin and Hold_Margin to zero and solving for the minimum and maximum etch delays allows the range of allowable etch to be defined.

Max_Etch <= Cycle_Time - Max_Clk2out - Setup_Time – Setup_Clock_Skew

Min_Etch >= Hold_Time + Hold_Clock_Skew - Min_Clk2Out
Terms:

- Cycle Time: Time of 1 clock cycle in nanoseconds
- Max_Clk2out: Maximum propagation delay time of a component (driving a standard load) from a clock edge to data valid
- Min_Clk2out: Minimum propagation delay time of a component (driving a standard load) from a clock edge to data valid
- Setup Time: Time that a component requires input data to be valid before the clock to that component becomes valid.
- Hold Time: Time that a component requires input data to be valid after the clock to that component becomes valid.
- Setup_Clock_Skew: Clock skew that affects setup transfers
- Hold_Clock_Skew: Clock skew that affects hold transfer
- Max_Etch: Maximum Interconnect_Delay
- Min_Etch: Minimum Interconnect_Delay

Example

To demonstrate this methodology, a sample network from a broadband network processor is used. Figure 4 shows the network topology for a network processor that communicates to 2 MAC (Media Access) devices. In this example there are eight variables that are being analyzed and we need information at three operating frequencies. This means that 768 simulations would need to be run to cover all possible cases. Using the Solution Space Methodology, we break out the SSO, ISI, and crosstalk simulations. The ISI analysis

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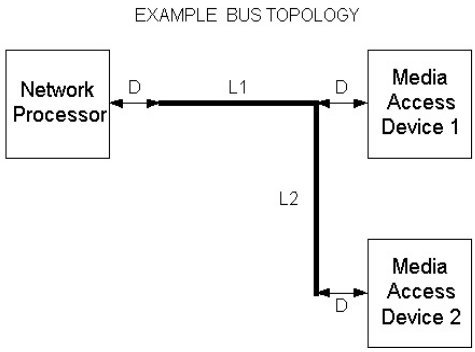
determines the depth of the simulation pattern and if the signal properties are independent of the operating frequency. In the example presented, ISI is shown to not be a factor and that the same delay information can be used to compute the timing margins at all frequencies of interest. For the example, the methodology provides a 10x reduction in the number of simulations needed to accurately simulate the design space.

Figure 4



Solution Space Methodology Setup

The following specifications defined the variables applied to the solution space simulations:

- Board Impedance: Design targets were specified as Zo = 50 ohms, Tpd = 180ps/in. Given the manufacturing tolerances associated with PCB fabrication, Slow etch and Fast etch models were created.
    - Fast etch was defined as: Zo = 55, Tpd = 160ps/in
    - Typical Etch was defined as: Zo = 50, Tpd = 180ps/in
    - Slow etch was defined as: Zo = 45, Tpd = 200ps/in

- Crosstalk /spacing rules: All routing was performed at 5mil width, 5mil space as specified by existing layout.
- Board Stackup: Spice simulations assumed that signal interconnect was performed in a stripline environment. It was also assumed that signal crosstalk was caused only by etch on the same layer.
- Topology Rules: Routing was performed in a daisy-chain fashion as specified by the module layout. 0.5 inches of dispersion etch was included to escape each package.
- Length Rules: The following network topologies were explored as part of the Solution Space Analysis:
    - L1 = 1.0 inches, L2 = 1.0 inches, D = 0.5 inches
    - L1 = 1.0 inches, L2 = 2.0 inches, D = 0.5 inches
    - L1 = 2.0 inches, L2 = 1.0 inches, D = 0.5 inches
    - L1 = 2.0 inches, L2 = 2.0 inches, D = 0.5 inches

- Signal Quality Limits:
    - Overshoot Limit 4.3V
    - Undershoot Limit -0.8V
- Frequencies: Simulations and timing analysis were performed at 66.667MHz, 83.333MHz, and 104.000MHz
- Environment: Voltage and temperature limits were as follows:
    - Worst Case: 100c, VDD_IO = 3.0V, VDD_Core = 1.9V, SS silicon models
    - Best Case: 0c, VDD_IO = 3.6V, VDD_Core = 2.1V, FF silicon models

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Results

The solution space data and the resulting timing analysis are based upon the entire range of network configurations. Process simulations covered 2 design corners, best case and worst case. The best case corner included the fast silicon, fast etch, and best case environment. The worst case corner includes slow silicon, slow etch, and worst case environment. All combinations of etch lengths were simulated. In addition simulations were run to examine SSO, Crosstalk, and ISI affects. The results of the SSO simulations are used in the final timing analysis to adjust the components AC spec. The Crosstalk results are used to adjust the switching points used to calculate the interconnect delay. The ISI simulations were performed to determine the type of input stimulus needed.

Clock Skew Analysis

The clock system utilizes a radial distribution from a single clock buffer. All clocks are routed on the same module layer and are all the same length. This results in there being no etch skew contribution to clock skew. A jitter budget of 200ps and 300ps of output to output skew was allowed for the clock source. This results in the following:

- Setup_Clock_Skew (any source to any target) = 0.5ns
- Hold_Clock_Skew (any source to any target) = 0.3ns

ISI Analysis

Spice analysis showed that the settling time of the bus was 8 ns. This means that ISI does affect this bus at speeds greater than 125MHz. Since this design is specified to operate at less than 125MHz, ISI is not an issue. For completeness in this example, the complex waveform shown in Figure 5 was used for Hspice simulation.

Crosstalk Analysis

The crosstalk analysis used a modeling strategy that had four aggressors and one victim. The crosstalk analysis showed 200mV of noise when the aggressor nets are switching. To ensure proper timing with crosstalk affects, the following waveform measurement points are used:

- Rising Data Setup: Vswitch + 200mV
- Rising Data Hold: Vswitch – 200mV
- Falling Data Setup: Vswitch – 200mV
- Falling Data Hold: Vswitch + 200mV

The Evaluation board was routed with 5/5 technology (5 mil wide etch, 5 mil space between etches). This routing spacing is susceptible to crosstalk noise. With the edge rates seen in simulation, each 100mV of crosstalk translates into 100ps of additional timing delay. While not required for 66 or 83MHz operation, routing at wider pitch, 5/10 or 5/15, will reduce interconnect delays.

Signal Quality

The analysis was done with an Overshoot Limit of 4.3V and an Undershoot Limit of -0.8V. These limits were checked at each source and target. In addition the waveforms were examined for ringback, signal slewrate, and monotinicity. A review of the signal quality found no issues that would affect device reliability or degrade system noise margin.

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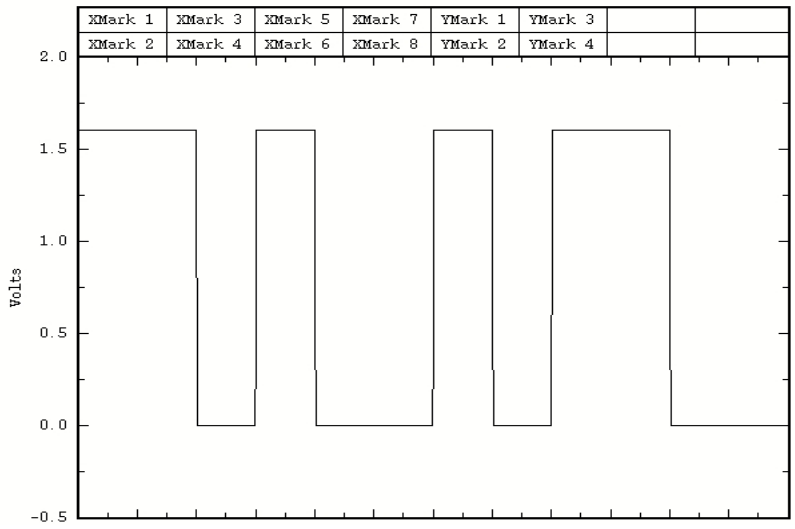
Figure 5



Interconnect Delays

Applying the noise margins determined by the crosstalk analysis and the Hspice stimulus defined by the ISI analysis, the Solution Space Analysis returned the data for the interconnect delays. This data was captured for bus operation at 66MHz, 83MHz, and 104MHz and is presented in Table1, Table2, and Table 3 respectively. As can be seen from the data, interconnect delay was independent of frequency, thus demonstrating that ISI was not a factor in these nets.

Timing Results

Utilizing the Clock skew, Interconnect delay, the component AC specs (defined in Table 5), and the target operating frequency, the setup and hold margins of the design can be calculated. Table 4 summarizes the results of this investigation.

Clock Skew Correction

The results of this table show that by applying a clock skew of approximately 1ns between the network processor and the two macs, this bus can operate properly at frequencies up to 83MHz. Operation at higher frequency will require improvements to the device AC specifications and interconnect delay properties.

Summary

For complex, high-speed networks, there are many device conditions that must be simulated. The Solution Space Methodology breaks the design down into a number of manageable tasks that can be done independently. These smaller tasks result in fewer overall simulations and it is our contention that the adoption of the Solution Space Methodology allows the designer to provide a through analysis of complex high speed networks with greater productivity than traditional methods.

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TABLE 1

Network Delays at 66MHz Operation				
	Min Rise	Max Rise	Min Fall	Max Fall
Network Processor to MAC1	0.486	1.656	0.692	1.071
Network Processor to MAC2	0.839	1.407	0.881	1.194
MAC1 to Network Processor	0.911	2.006	0.545	1.089
MAC2 to Network Processor	1.199	2.126	0.850	1.505

TABLE 2

Network Delays at 83MHz Operation				
	Min Rise	Max Rise	Min Fall	Max Fall
Network Processor to MAC1	0.487	1.644	0.697	1.071
Network Processor to MAC2	0.844	1.397	0.881	1.205
MAC1 to Network Processor	0.915	1.980	0.544	1.102
MAC2 to Network Processor	1.186	2.118	0.850	1.525

TABLE 3

Network Delays at 104MHz Operation				
	Min Rise	Max Rise	Min Fall	Max Fall
Network Processor to MAC1	0.491	1.694	0.697	1.071
Network Processor to MAC2	0.845	1.440	0.881	1.210
MAC1 to Network Processor	0.914	1.994	0.545	1.122
MAC2 to Network Processor	1.201	2.116	0.850	1.539

TABLE 4

Transfer	Freq. (MHz)	Setup Margin (ns)	Hold Margin (ns)
NetProc to MAC1	66	2.494	2.191
	83	-0.494	2.191
	104	-2.929	2.191
NetProc to MAC2	66	2.743	2.545
	83	-0.247	2.545
	104	-2.675	2.545
MAC1 to NetProc	66	4.494	3.245
	83	1.520	3.245
	104	-0.879	3.245
MAC2 to NetProc	66	4.374	3.550
	83	1.382	3.550
	104	-1.001	3.550

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Table 5 defines the component AC specifications applied in the timing analysis of the Evaluation board.

TABLE 5

	Min	Max	Units
NetProc CLK2OUT	2.00	6.35	ns
NetProc SETUP	3.00		ns
NetProc HOLD	0.00		ns
MAC1 CLK2OUT	3.00	5.00	ns
MAC1 SETUP	4.00		ns
MAC1 HOLD	0.00		ns
MAC2 CLK2OUT	3.00	5.00	ns
MAC2 SETUP	4.00		ns
MAC2 HOLD	0.00		ns

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