



IBIS Advanced Technology Modeling Group (IBIS-ATM)* Status Report

Todd Westerhoff, SiSoft
DesignCon IBIS Summit
Feb 1, 2007

* Formerly IBIS-Macro



Signal Integrity Software, Inc.

Agenda

- Updated Group Charter
- Peak Distortion Analysis
- HSpice investigations
- Cadence's Proposal / BIRD
- Circuit vs. Signal Simulation
- DLL / Executables / Encrypted Source, AMS / SystemC / Other Languages
- Terminology Presentations
- Current Status

Updated Group Charter

- Changed name to IBIS Advanced Technology Modeling Group (IBIS-ATM)
- Current goal:
 - Define a transmitter/receiver modeling standard for SERDES channel analysis that encompasses equalization and clock recovery
- The solution must:
 - Support multiple EDA vendors
 - Support multiple IC vendors
 - Protect semiconductor vendor IP
 - Support combined transmitter/receiver design
 - Support design optimization

Peak Distortion Analysis

Worst-case Received Voltage Difference (RVD) for WC0

Reference
Worst-case 0

$$V_{wco} = \sum ISI+$$

$$RVD_{wco} = V_{reference} - V_{wco} = \left[\frac{cursor + \sum ISI}{2} \right] - [\sum ISI+]$$

$$= \frac{cursor}{2} + \frac{\sum ISI+}{2} + \frac{\sum ISI-}{2} - \sum ISI+ = \frac{cursor}{2} - \frac{\sum ISI+}{2} + \frac{\sum ISI-}{2}$$

$$= \frac{cursor}{2} - \frac{\sum |ISI+|}{2} - \frac{\sum |ISI-|}{2} = \frac{cursor}{2} - \frac{\sum |ISI|}{2}$$

Peak Distortion Analysis
Brian Cooper, CRL
January 22, 2007

- Analytical method for predicting maximum eye closure based on channel pulse response
- Implemented in VHDL-AMS and demonstrated by Arpad Muranyi of Intel


Reference presentation:

http://download.intel.com/education/highered/signal/ELC T865/Class2_15_16_Peak_Distortion_Analysis.ppt

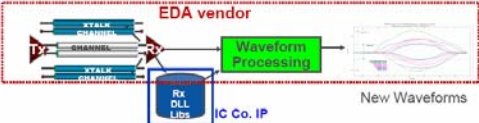
HSpice Investigations

- Request from Cadence at Asian IBIS Summit to extend [External Model] Spice syntax to allow parameter passing
 - Berkeley Spice [currently supported] does not provide this
- Asked Synopsys if they would make HSpice syntax publicly available [de facto standard]
 - Synopsys declined, not wanting to restrict future extensions to HSpice's syntax
- Issue currently considered closed
 - Open invitation to group to propose specific syntax for parameter passing



Cadence's AMI Proposal

Proposed Solution & Architecture 

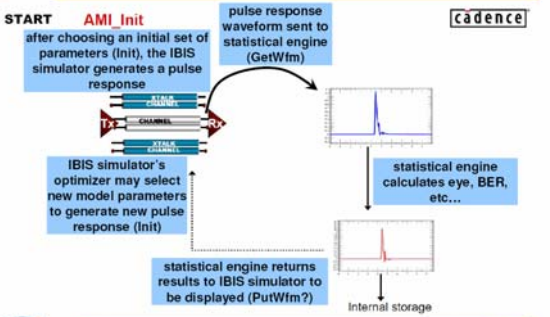
- Allow IC companies to develop "executable" algorithm based models that plug into the simulator through a dynamically linked library (dll)
- Simplest possible public API (C-wrapper)
- Algorithmic Models in a dll
 - Can capture and encapsulate complex algorithms
 - Can add jitter
 - Can include CDR modules
 - Protects IP without tool-specific encryption, no simulator specific encryption needed
 - Provides SERDES and EDA vendor independent interoperability if standardized
 - Can complete measurement loop - pluggable soft IP



- Multiple presentations at:
 - http://www.vhdl.org/pub/ibis/macromodel_wip/
- Ongoing discussions of Cadence's proposal and algorithms therein
- Related discussions on details of channel characterization and modeling
- Cadence presented proposal as draft IBIS BIRD

 **Kumar's optimization loop (annotated)** 

START AMI_Init
after choosing an initial set of parameters (Init), the IBIS simulator generates a pulse response





IBIS simulator's optimizer may select new model parameters to generate new pulse response (Init)

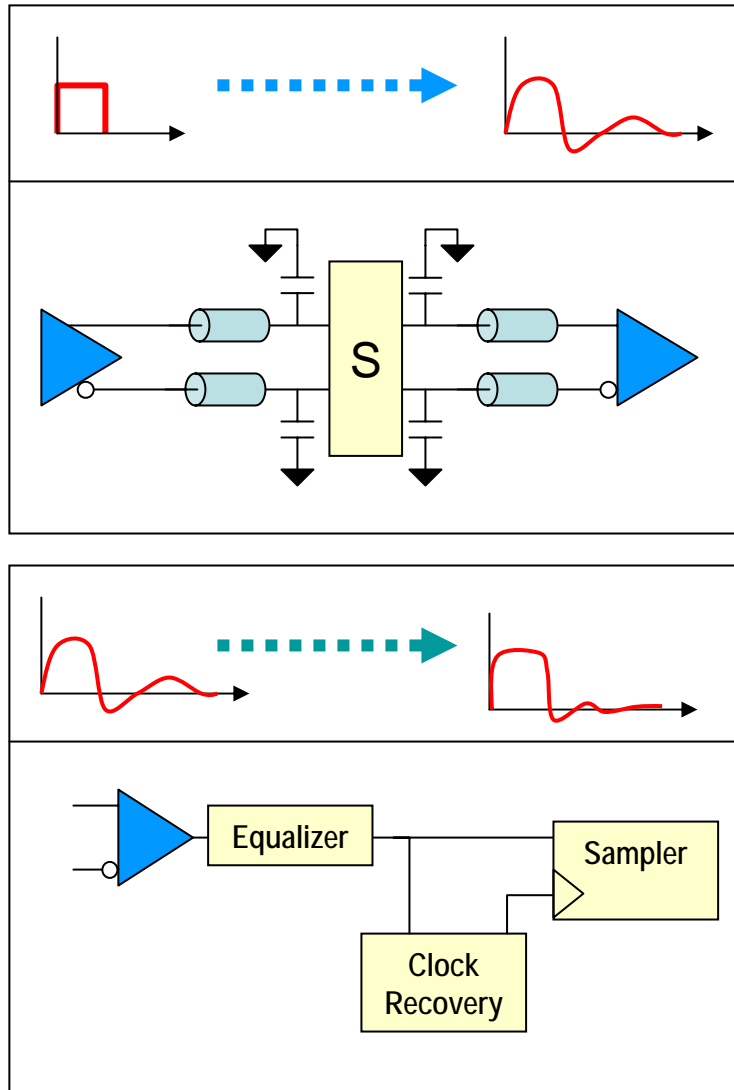
statistical engine returns results to IBIS simulator to be displayed (PutWfm?)

statistical engine calculates eye, BER, etc...

Internal storage

 *Other brands and names are the property of their respective owners.  Page 5

Circuit Simulation vs. Signal Processing

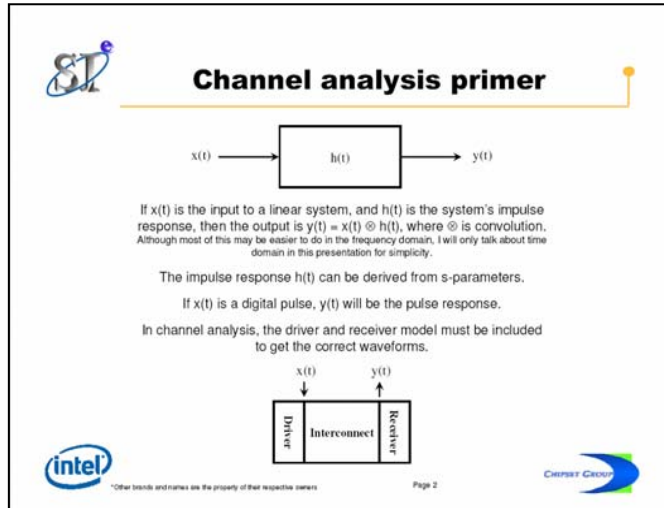


- Circuit Modeling/Simulation
 - Interconnect models
 - Network characterization
 - Impulse Response
 - Pulse Response
- Signal Processing Analysis
 - Transmitter equalization
 - Receiver equalization
 - Time-domain waveform generation (convolution)
 - Clock recovery

DLL / Executables / Encrypted Source, AMS / SystemC / Other Languages

- Secondary / deployment issue
- Extensively discussed model development and distribution:
 - Tradeoffs between different development languages
 - System language trends
 - Advantages / disadvantages of different distribution methods (.dll vs. executable vs. encrypted source)
 - Strengths and weaknesses of different IP-protection schemes

Terminology Presentations



Channel analysis primer

$x(t) \rightarrow [h(t)] \rightarrow y(t)$

If $x(t)$ is the input to a linear system, and $h(t)$ is the system's impulse response, then the output is $y(t) = x(t) \otimes h(t)$, where \otimes is convolution. Although most of this may be easier to do in the frequency domain, I will only talk about time domain in this presentation for simplicity.

The impulse response $h(t)$ can be derived from s-parameters.
If $x(t)$ is a digital pulse, $y(t)$ will be the pulse response.

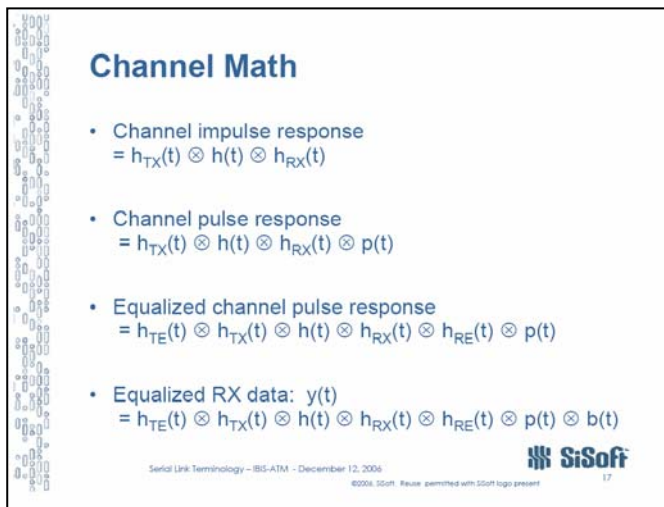
In channel analysis, the driver and receiver model must be included to get the correct waveforms.

$x(t)$ $y(t)$
↓ ↑
Driver Interconnect Receiver

intel *Other brands and names are the property of their respective owners. Page 2 CEMIST Group

- Intel

- http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20061024/arpadmuranyi/Channel%20analysis%20flow%20with%20IBIS/IBIS_API_flow.pdf
- TinyURL version:
 - <http://tinyurl.com/238mdw>



Channel Math

- Channel impulse response
= $h_{TX}(t) \otimes h(t) \otimes h_{RX}(t)$
- Channel pulse response
= $h_{TX}(t) \otimes h(t) \otimes h_{RX}(t) \otimes p(t)$
- Equalized channel pulse response
= $h_{TE}(t) \otimes h_{TX}(t) \otimes h(t) \otimes h_{RX}(t) \otimes h_{RE}(t) \otimes p(t)$
- Equalized RX data: $y(t)$
= $h_{TE}(t) \otimes h_{TX}(t) \otimes h(t) \otimes h_{RX}(t) \otimes h_{RE}(t) \otimes p(t) \otimes b(t)$

Serial Link Terminology – IBIS-ATM - December 12, 2006
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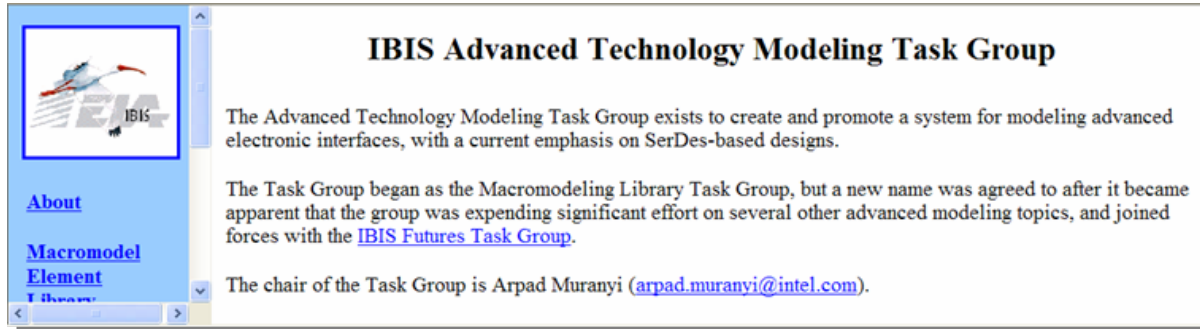
- SiSoft

- http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20061212/toddwesterhoff/Serial%20Link%20Terminology/serial_link_terminology.pdf
- TinyURL version:
 - <http://tinyurl.com/yuhxn9>

Current Status

- Still need better definition of target audience
 - Silicon/circuit designers?
 - Model developers?
 - System designers?
- Network characterization terminology still unclear
 - Impulse response vs. pulse response vs. transfer function vs. pole/zero representations
- Cadence's proposal under review
 - Ongoing discussions of detailed implications
 - SiSoft recommendations for enhancement
 - Mechanism to publish model parameters for EDA tool
 - Need analysis methodology-independent models
- Still exploring different analytical approaches

For More Information



- IBIS-ATM / IBIS-Macro Website
 - www.eda.org/pub/ibis/macromodel_wip/
- IBIS-Macro mail reflector
 - Mail to: ibis-macro-request@freelists.org
 - Subject: subscribe
- IBIS-Macro mail archives
 - www.freelists.org/archives/ibis-macro