Quantum-SI™ (QSI) automatically determines setup/hold and voltage margins for high-speed parallel design through integrated signal integrity and timing analysis. Automated pre-route design space exploration optimizes design performance, reliability and cost, while real-time post-route validation analyzes an entire system overnight to ensure designs are ready for fab-out. Advanced modeling, simulation and waveform processing techniques determine design margins more quickly and accurately than traditional signal integrity tools.

ANALYZE YOUR ENTIRE INTERFACE AT ONCE

Quantum-SI analyzes an entire parallel interface for compliance with both timing and signal integrity constraints. Each net class is analyzed using its own clock/data rate, stimulus, transaction-dependent drive strength, transaction-dependent termination settings and timing reference points. Simulation waveforms are automatically processed to validate waveform quality and extract interconnect delays based on interface protocols, with full support for DDR4/5 and other popular standards. Every net in the entire interface is automatically set up, simulated and postprocessed.

The Quantum-SI timing analyzer creates a comprehensive report of the design’s timing and voltage margins. This report details the margin associated with every signal integrity and timing constraint across the entire interface and includes multiple levels of drill-down detail. Quantum-SI reduces design time and costs by performing sophisticated design analysis quickly and automatically.

FLEXIBLE, ACCURATE MODELING

Quantum-SI models topologies at multiple levels of detail based on your interface’s operating voltage and timing margins. I/O buffers can be modeled at either the behavioral (IBIS) or detailed transistor (HSPICE) level. Device packages can be represented as IBIS, SPICE subcircuit or S-parameter descriptions.

Comprehensive timing models define component input and output timing characteristics. Dynamic timing models support today’s latest adaptive timing technologies.

Accurate noise modeling is a key requirement for accurately assessing system operating margins. Quantum-SI employs a unique pre-/post-layout methodology for modeling switching noise and crosstalk that allows noise budgets to be established early in the design cycle and rapidly validated after layout.

INTEGRATED PRE-/POST-LAYOUT ANALYSIS

The Quantum-SI schematic editor graphically displays each net class in the interface, allowing its properties to be managed graphically. During pre-layout analysis, designers modify net classes to reflect their intended routing strategies, and QSI automatically determines voltage and timing margins. Designers sweep interconnect and I/O parameters during simulation to determine their effect on design margins. Hundreds of design tradeoffs are automatically analyzed to select the optimal set of design rules for cost, performance and reliability.

Quantum-SI provides superior post-route automation, allowing designers to run nightly post-route SI regressions of their design as PCB layout progresses. QSI uses prereoute setup information to automatically identify net classes in routed databases and run simulations. Quantum-SI presents signal integrity and timing results in the same formats as pre-route analysis, simplifying comparison of actual to expected results.

Quantum-SI imports PCB databases from multiple CAD systems, guiding users through the process. PCB databases can be displayed graphically, zooming and highlighting problem areas automatically.
COMPREHENSIVE WAVEFORM PROCESSING

Generating thousands of simulation cases is easy, but extracting accurate waveform quality and interconnect delay information is not. Quantum-SI analyzes signals at the device pin, pad, or core using the most rigorous waveform processing in the industry. Every edge of every waveform is analyzed for waveform quality, slew rate, area and timing parameters. Interconnect delays are automatically normalized based on component timing specifications, including full derating support for DDR4/5 and other standards.

ADVANCED SIMULATION RESULTS VIEWER

SiViewer provides comprehensive, interactive display of simulation results. Waveform data is presented in time-domain, eye diagram and bus (side by side) formats, with key waveform metrics and constraint violations annotated on the waveform display. Hundreds of waveforms can be plotted quickly, scaled, measured, annotated and saved for inclusion in design reports.

Signal integrity / timing analysis results can be displayed as scatter plots, showing how voltage and timing margins are distributed across an entire interface, allowing design trends and problem areas to be identified quickly.

QUANTUM-SI DESIGN KITS

Quantum-SI Design Kits are ready-to-run setups for popular interface standards such as DDR4/5 that can save weeks in your next design cycle. Design kits include validated signal integrity/timing models, reference topologies and constraint checks – just edit topologies to reflect your proposed routing strategies and let Quantum-SI determine your voltage and timing margins.

Quantum-SI Design Kits are available at three levels of customization:

- Architectural (technology-specific with generic components)
- Implementation (complete pre-route setups for specific components)
- Validation (complete pre-/post-route setups based on reference PCB designs)

BACKED BY SiSoft’s EXPERIENCE IN HIGH-SPEED SYSTEMS DESIGN

SiSoft’s staff of recognized industry experts keeps SiSoft’s products at the forefront of high-speed design by using them every day to perform state-of-the-art design and analysis. SiSoft provides a full range of model development, design analysis and methodology training services. Let SiSoft help you make your next design successful with our unique blend of tools, methodology training and support.

CAD LAYOUT SYSTEM SUPPORT

Allegro®, Expedition PCB™, PADS, Board Station®, Pantheon®, Altium Designer, Zuken CR-5000/8000 and CR-8000, ODB++, EBD

To learn more about SiSoft’s products, contact sales@sisoft.com or visit our website at www.sisoft.com.