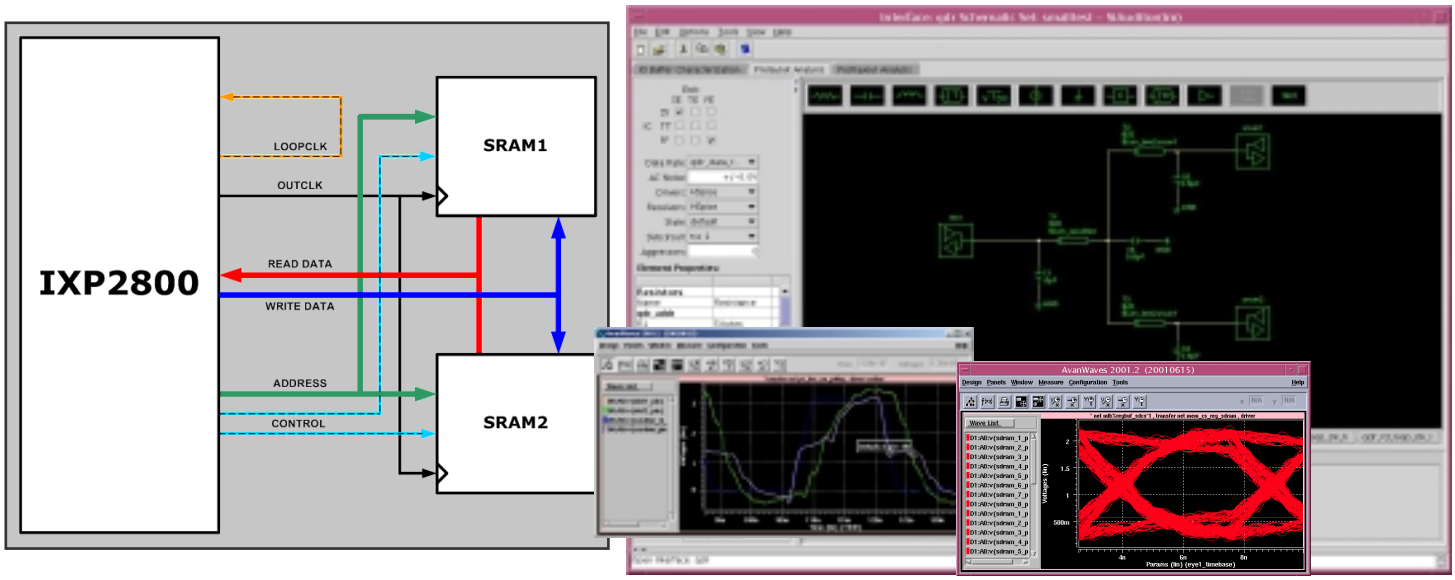
Quick Turn Signal Integrity and Timing Analysis



Signal Integrity and Timing Analysis Couldn't be Easier!

Overview

An increasing number of companies are experiencing sharp upturns in system-level signal integrity and timing issues that result in project delays and increased development cost. Many of these companies do not have in-house signal integrity analysis expertise. Other companies that do possess this expertise may periodically need to outsource overflow work.

To address these industry needs, SiSoft created Quick Turn Signal Integrity (QTSI) analysis service packages to make signal integrity expertise available at very affordable prices. SiSoft is offering low cost pre-layout analysis and post-layout verification service packages for standard interface configurations. QTSI is presently available for AGP, PCI, PCI-X, DDR-SDRAM, SDRAM, DDR-SRAM, QDR-SRAM, SPI-3, SPI-4, and HyperTransport interfaces.

QTSI Process

SiSoft's QTSI analysis service is easy to use—customers follow simple step-by-step instructions to initiate the pre- or post-layout quick turn process. SiSoft provides customers with a QTSI kit, including instructions, questionnaires and templates. Customers send completed questionnaires to SiSoft—SiSoft returns a quote within two business days.

Once customers approve quotes and send the completed templates to SiSoft, the analysis process is initiated. After completing the analysis, SiSoft provides customers with an analysis report and results for each analyzed interface. SiSoft's consultants also schedule a telecon to debrief customers on the analysis results.

Major Service Package Benefits

- Provides access to industry experts for companies that don't have in-house signal integrity expertise
- Flexible and easy to use
- Provides a reliable source of low cost pre-layout analysis and post-layout verification for standard interface configurations
  - Fixed fee for basic design configurations
  - Low cost add-on options available to tailor analysis to meet specific customer needs
- Use of Core-to-Core™ analysis methodology ensures accurate prediction of system-level margins
  - Analysis results include the integrated effects of signal integrity and timing
  - Analysis is performed with the most rigorous waveform and eye diagram processing available over the desired solution space
  - Every edge of every waveform is processed and analyzed to determine waveform quality and timing margins
- Supports most major PCB layout flows
- Accommodates databases from different layout products for post-layout verification of multi-board systems

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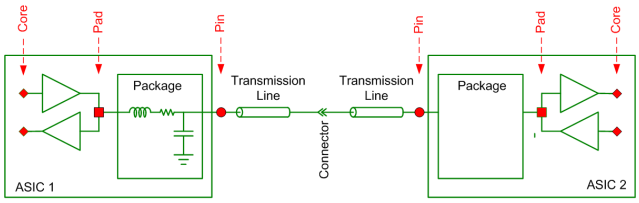
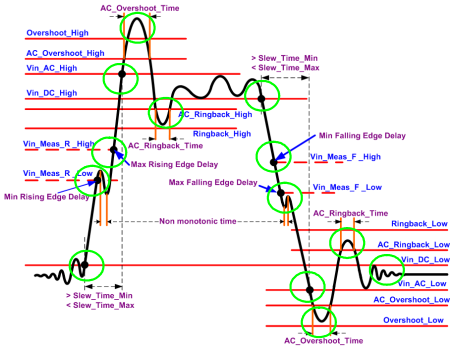
QTSI Analysis Methodology

SiSoft's products are used to perform all pre-layout and post-layout analysis. Core-to-Core™ methodology provides a formalized process for analyzing signal integrity and timing from the inputs of output buffers to the outputs of input buffers and all the electrical interconnects in between.



Analysis is performed with the most rigorous waveform and eye diagram processing available, over process, voltage, and temperature for two corner conditions. Every edge of every waveform is analyzed at up to 18 levels (see figure below) to determine waveform quality and timing margins.



Waveforms are analyzed for the effects of static and dynamic overshoot, ring back, monotonicity, logic level noise margin, slew rate, and to capture switching threshold data for timing analysis. Static timing analysis is performed on the processed data to determine setup and hold margins for synchronous, source-synchronous and clock recovery interfaces.

Basic QTSI Pre-Layout Analysis Package

The basic pre-layout interface configuration includes the items listed in the following table.

Item Description	Included in Basic Design Configuration for Each Interface
Unique IBIS Component Models	**2**
Devices on Interface Bus	**5**
Unique Interface Topologies	**1**
Simulation Cases x Corner Conditions	**600**
Number of Circuit Elements	**80**
Solution Space Variables	**50**

Additional analysis options may be added to basic analysis packages for incremental fees. Options include additional models, devices, interface topologies, simulation cases, circuit elements, solution space variables, corner conditions, part variants, populations, bus turnaround analysis, and coupling analysis.

Basic QTSI Post-Layout Verification Package

The basic post-layout interface configuration includes the items listed in the following table.

Item Description	Included in Basic Design Configuration for Each Interface
Unique IBIS Component Models	**2**
Devices on Interface Bus	**5**
Boards to be Analyzed	**1**
Corner Conditions Included	**2**

Additional verification options may be added to basic analysis packages for incremental fees. Options include additional models, devices, boards, corner conditions, part variants, populations, bus turnaround analysis, and crosstalk analysis.

Summary

SiSoft's integrated signal integrity and timing analysis approach provides customers with unprecedented accuracy in predicting realistic worst-case system margins. Accurate prediction of system margins allows customers to:

- Reduce the risk of integrating the latest high-speed interface technologies into their products.
- Efficiently allocate margins to reduce product cost and complexity *(e.g., eliminate parts, reduce board layers, and use less expensive parts).*

SiSoft's QTSI service packages provide customers with high-quality signal integrity and timing analysis at very affordable prices. QTSI service packages are designed to help customers get reliable, cost-effective products to market quicker while lowering development cost.

Contact SiSoft

To learn more about "Quick Turn" signal integrity service packages, contact sales@sisoft.com or visit our website at www.sisoft.com.

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